quantumdata 980 Firmware & External Manager v5.38 Release Notes

August 16, 2019 ver. 2

1 Overview

This document provides information on Release 5.38 of the firmware and External Manager software for the quantumdata 980B and 980R Advanced Test Platforms. Included are changes made since the previous Full Release, version 5.30.

Release 5.38 features **DisplayPort DSC Compliance Tests** in support of VESA Normative Testing requirements for products using **Display Stream Compression with DisplayPort**. Please follow this link to the appendix for details on VESA DP DSC Compliance Test support in this release.

The appendix also contains reference tables for DisplayPort Link Layer Compliance support, HDMI FRL Compliance support, and HDMI eARC Compliance support.

For HDMI 2.1 FRL, 5 new Protocol Compliance Tests are added, and 22 new format timings/lane combinations are added for pixel rates above 1188 MHz.

For DisplayPort 1.4, six new DSC Compliance Tests are added. For details on these new features, please continue reading this document.

For further information on the quantumdata 980 system, please refer to the Quick Start Guide for the 980 Advanced Test Platforms, and the User Guides for the individual modules, all available on our website at https://www.quantumdata.com

2 Installation Instructions

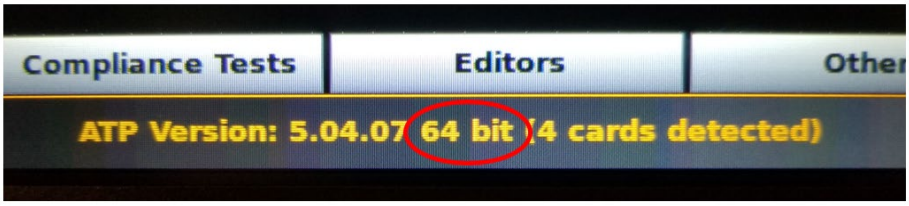
Important Note: When upgrading the 980 system firmware, please be sure to disconnect any video cables that are connected to the 980 Protocol Analyzer / Video Generator modules. Failure to do so may result in issues during upgrade.

Begin by installing the **Windows External Manager** software:

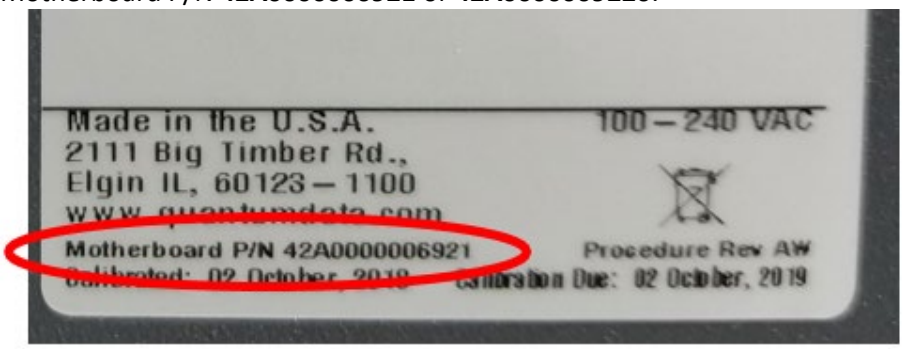
1. Download the **Windows External Manager 5.38** file R_980mgr_5.38_Win32.msi
2. Double-click or Run this file to install it.

Then install the Instrument Firmware **Release**.
Important Note: 2 different versions of the Instrument Firmware are available, for 32-bit and for 64-bit operating systems. You must install the correct version for your specific 980. (The incorrect version will be refused during the upgrade process.) Please make one or both of the following checks to determine whether you need the 64-bit firmware:

1. At the bottom of the instrument Card Control screen, check for “64 bit” indication:



2. On the product label on the back (980B) or bottom (980R) of the instrument, check for Motherboard P/N **42A0000006921** or **42A0000009220**:



If the ATP version shows 64 bit, or if the label shows either of the above part numbers, then download the “980-atp-64” firmware. Otherwise, you have a 32-bit system, so download the “980-atp-32” firmware.

1. Download the release “980-atp-xx” .deb firmware file as indicated above.
2. Launch the newly installed External Manager (980 Manager) and connect to the 980 via Ethernet TCP/IP. (For information on the 980 network connections, please refer to the Advanced Test Platform Quick Start Guide and related erratum below.)
    a. Note: you may see a warning about version mismatch. This is normal and indicates that you should continue with the version upgrade before using the instrument with the new version of the External Manager.
3. From the External 980 Manager program, pull down the **Instrument** menu and select **Upgrade UI/Firmware/Gateware**. Browse to and select the 980-atp-xx release file, select **Open**, and continue with the process. The 980 will power down at the end.

If the 980 is licensed for **HDR Lab Images** (License 45):

4. Download the HDR Lab Images .deb file.
5. From the External 980 Manager program, pull down the **Instrument** menu and select **Upgrade System Components**. Browse to and select the hdr-lab-images.deb file, select Open and continue with the process.

If the 980 is licensed for **HDMI HDCP CTS 2.2 Compliance Test for Sinks** (License 29):

6. Download the 980-hdcp2-sink-ct.deb file.
7. From the External 980 Manager program, pull down the **Instrument** menu and select **Upgrade CT Scripts**. Browse to and select the 980-hdcp2-sink-ct.deb file, select Open and continue with the process.

If the 980 is licensed for **HDMI CTS 1.4b Compliance Test for Sinks** (License 6) or **HDMI CTS 2.0 Package 4 Sink Tests** (License 27):

8. Download the 980-hdmi-sink-ct.deb file.

9. From the External 980 Manager program, pull down the **Instrument** menu and select **Upgrade CT Scripts**. Browse to and select the 980-hdmi-sink-ct.deb file, select Open and continue with the process.

To verify the installation:

1. After installing any necessary packages from above, press the front button and Reboot the 980.
2. After the reboot, view the Instrument Information report in one of the following ways:
    a. From the External 980 Manager, when connected to the 980, pull down the **Instrument** menu and select **Information**.
    b. From the External 980 Manager, when connected to the 980, locate the **Instruments** section in **Navigator**, right-click on the instrument, and select **Information**.
    c. From the 980-front panel touch screen, select the **Other** page and then select **About the 980 Manager**.
3. Verify the following version information from the Instrument Information report, for the specific versions of modules installed:

Table 1: Module revisions and Build Versions

Module	FPGA Versions (Changes compared to previous release are in GREEN)	
	980	
	5.30	5.38
DP 1.2 980 Protocol Analyzer Rev D	4.17.85 Build Number: 1	**4.17.85 Build Number: 1**
DP 1.2 980 Protocol Analyzer Rev E	4.17.85 Build Number: 1	**4.17.85 Build Number: 1**
DP 1.2 980 Protocol Analyzer Rev E (410)	4.18.42 Build Number: 1	**4.18.42 Build Number: 1**
DP 1.2 980 Protocol Analyzer Rev F	4.18.62 Build Number: 1	**4.18.62 Build Number: 1**
DP 1.4 980 Protocol Analyzer	4.25.218 Build Number: 1	**4.25.227 Build Number: 1**
DP 1.4 USB-C 980 Protocol Analyzer	4.26.32 Build Number: 1	**4.26.54 Build Number: 1**
SDI Scope	4.33.7 Build Number: 32	**4.33.7 Build Number: 32**
HDMI 2.0 980 Video Generator Rev B	4.34.1 Build Number: 32	**4.34.1 Build Number: 32**
HDMI 2.0 980 Video Generator Rev C	4.34.1 Build Number: 32	**4.34.1 Build Number: 32**
HDMI 1.4 980 Protocol Analyzer	4.22.1 Build Number: 57	**4.22.1 Build Number: 57**
HDMI 2.0 980 Protocol Analyzer	4.22.7 Build Number: 43	**4.22.7 Build Number: 43**
HDMI 2.0 RX/TX	4.27.1 Build Number: 55	**4.27.1 Build Number: 55**

HDMI 2.1 RX/TX	5.30.1 Build Number: 173	**5.40.8 Build Number: 115**
Phy and Protocol Aux Channel Analyzer	5.16.24 Build Number: 12	**5.16.24 Build Number: 12**

3 New and Improved Features and Functions

3.1 New HDMI 2.1 FRL video timings: pixel rates greater than 1188 MHz.

This applies to a 980B or 980R that contains the HDMI 2.1 48Gb/s Analyzer/Generator module (95-00156) and the HDMI 2.1 TMDS/FRL Video Generator option (95-00158, license 52.)

Release 5.38 adds a large number of FRL timing/lane/pixel subsampling combinations.

3.2 Added 6 new HDMI 2.1 FRL Protocol Compliance Tests

Release 5.38 adds the following Fixed Rate Link (FRL) Compliance Tests for total of 39 Tests of Source Devices and 27 Tests of Sink Devices:

FRL Compliance Tests of Sink Devices:

Deep Color Timing
HFR2-16: Sink Video Timing (FRL Mode) – 4320p Deep Color

Sink EDID Testing
HFR2-70: Sink EDID – HF-VSDB Reserved Bits

FRL Compliance Tests of Source Devices:

Protocol
HFR1-20: Source FRL Packets – FRL Control Periods
HFR1-23: Source FRL Protocol – Data Flow Metering Variations

8bpc Timing
HFR1-24: Source Video Timing (FRL Mode) –2160p 24-bit Color Depth

Source EDID Read Testing
HFR1-66: Source EDID Reading – VESA E-EDID 1.3

3.3 Added new DisplayPort 1.4 DSC Compliance Tests

Release 5.38 adds the following DP Display Stream Compression (DSC) Compliance Tests for total of 7 Tests for Source Devices and 26 Tests of Sink Devices:

DP DSC Tests of Sink:

5.6.1.22: DSC Native 4:2:0 color depth test
5.6.1.23: DSC Native 4:2:0 block prediction test
5.6.1.24: DSC Native 4:2:0 bits-per-pixel test
5.6.1.25: DSC Native 4:2:0 slice test
5.6.1.26: DSC Native 4:2:0 lanes test

DP DSC Tests of Source:

4.6.1.6: DSC PPS Native 4:2:0 flag verification

4 Enhancements and Corrections

4.1 Updates and fixes

Bug ID	Description
	HDMI FRL packing efficiency enhancements
	HDMI tri-byte rate > 1188 M/s
	Additional FRL source CTs (see section 3)
	Additional FRL sink CTs (see section 3)
2971	FRL Playback status typo
2735	HDMI HDCP2.2 3C-06 failing incorrectly
2664	hdcp2 commands fixes
2953	HDMI 2.1: FRL Playback Generator updates
2955	DP 4K image with a particular DSC config, displays bottom of image incorrectly.

2668	Issue with CEC 2.0 compliance for a source
2938	TAARampB pattern failure on 64-bit OS
2959	EDID CTS 8-1 reports no result for EDIDs > 4 blocks
2946	USB-C: Fast Link Training fails for 2/4 lanes with 8.10Gbps link rate
2823	DP1.4 Tx Audio reset
2852	eDP ALPM implementation
2926	DP 1.4 eDP Backlight AUX control
2931	DSC image generation with fractional BPP
2935	DP1.4 and DP1.2 MST added NAK on sideband messaging timeout
2937	Disable automatic DP Tx link training on HPD detection
2939	DP 1.4 DSC MISC0 Bits Per Component not derived from PPS
2945	DP 1.4 DPCD eDP_CONFIGURATION_CAP register (address 0x0D) in none eDP mode
2948	DP 1.4 RX FEC error real-time status monitoring
2947	Corrected possible file loss when canceling a file move between 980 and PC
2927	GUI: Added eDP registers to DPCD Editor
2905	HDMI 2.0 pscope has incorrect video metrics
2917	HDMI Tx: Clearing HDMI forum VIC in command line does not clear it in the VSIF
2901	980 Manager import hex EDID file
3079	DP1.2 Rev C module system recognition issue

2982	HDMI 2.1 FRL source test results do not align with header
3076	eARC HFR5-1-57 test sometimes incorrectly fails
3065	HDMI 2.0 test HF1-15 fails incorrectly in some cases
2963	HDMI 2.1 Generator deep color HTOTAL correction
3004	Added image cache clean to the `sfd` command to clean up internal cache
2962	Fixed potential hang when running DP DSC realtime in loopback mode for a long time
2913	DP1.4: Ability to create/use Custom DSC Formats/Images
2912	DP1.4: switch between Synchronous and Asynchronous clocking DPTX
	Added interlaced support to HDMI 2.1 Tx
	Fixed issue with HDMI deep color
3083	Fixed HDMI 2.1 eARC ComplianceTest HFR5-1-27
	Added support for “high efficiency” packing in FRL
	Fixed HDMI 2.1 eARC HFR5-1-57 failing on CTA CA bits
	Fixed hvic (HDMI VIC) command for HDMI 2.0 Tx
3063	Fixed image DecodAdj for 64-bit OS
	Extended FRL support to 1782M rate
3048	Fixed distribution values for HDR10+ tests 10-13
3047	Fixed HDMI 2.1 eARC Compliance Test HFR5-1-51
3040	Allowed aspect ratio > 3 for HDMI 2.0 video generator

	Added checks to ensure TMDS fits within FRL lanes/rate
	Added latest CTA 861-G formats to generator
3027	Fixed HDR10+ test 11 for corner box duration
2978	Added command to allow any “animated” image to be frozen
1077	980 Added HDCP key status in Info Report
2885	980: Confusing Messages in HDMI 2.1 Source Compliance test HF1-52
2910	FRL Source HFR1_21 Compliance tests behavior when no data was captured
2942	Corrected error in HDMI 2.0 compliance test HF1-16
2981	FRL SRC CTS HFR1-27/29/30: Skip Image Analysis per CDF indication
3009	Improved error messaging for multiple FRL CT including HFR1-25
3014	HDMI 2.1 FRL Source test HFR1-15 clarifying error reporting
3015	Pixel depth analysis wrong for HFR1-18
3016	Improved error reporting detail for FRL CT HFR1-27
3032	FRL Source test HFR1-29 doesn't validate test image when required
3046	HFR1-14 does not handle interlace formats properly
2985	Added "Use Capabilities" option to the DP TX Backlight UI
3018	HDMI 2.1 Module generator: Enable the Compressed Audio UI.
2936	Added support for BT.2020 in DP.
3031	Added ability to search for a field in any CDF editor.

3002	Added new DPX import feature to the DP DSC UI.
3055	Fix DP spread spectrum toggle
2980	DP: Support split SDP in capture decode.
2973	HDMI2.1 FRL timing stats on the dashboard
2960	Change the EDID used in 7-33 test
2964	Support the ability to set the FRL rate to any rate on the HDMI 2.1 generator
2907	Added USB-C control UI to DP RX and TX
2808	Implement auto import of binary EDIDs when file signature is recognized
	Added some 1.4b formats to HFR2-14.
	Allow HDMI 2 EDID tests to be run on the 2.0 Rx/Tx card and the 2.1 card.
	Added an "Update Count" to the HDMI 2.1 realtime dashboard.
	Added 4:2:0 formats to HFR2-23 and 24
	Allow HF1-28 to cover all deep color modes.
	Added backlight status UI to DP/USBC RX
	Added "Error Info" panel to DP RX
	Added VSC capture to DP Real-time
	Added DP RX eDP enable/disable control

5 Errata

5.1 Known Issues

5.1.1 Power-on reboot - Important Notice!

Some quantumdata 980 systems exhibit occasional boot issue upon power-up from "cold" state.
In these occasions, the system enters an abnormal state where it continuously reboots at the BIOS level, instead of booting the 980 operating system and quantumdata application.
Solution: In the unlikely event that your 980 enters this state, please follow the simple steps below:

1. Turn off the main power rocker switch beside the mains power cord inlet (on the side of the 980).
2. Leave the system powered off for about 5 seconds.
3. Reapply power using the rocker switch and boot as usual.

These simple steps should get the system up and running. However, if this does not allow the 980 to boot normally, please contact us by referring to the Support section at the end of this document.

5.1.2 CEC Functionality on HDMI 18 Gbps RX/TX Analyzer receive port.

(2708) Regarding the HDMI 2.0 RX/TX analyzer (this is the HDMI 2.0 18 Gbps analyzer module that has 2 HDMI ports: Transmit and Receive): On this module, CEC is disabled by default on the HDMI Receive port. CEC functionality can be enabled temporarily (until the instrument is rebooted.) The following procedure will allow you to enable RX CEC functionality:

1. Launch the Windows External Manager (980 Manager) and connect to the 980.
2. From the Windows 980 Manager, select the **Other** GUI page.
3. Select the **Command Console**.
4. Select the **Connect** button.
5. Touch in the **Command** field to activate the touch screen keyboard.
6. Type the command **`discover`** and press **Enter**.
7. In the resulting list, locate the section that includes class: **Quantum Data, Inc. HDMI 2.0 RX/TX**.
8. Make note of the **slot** number indicated for this section. (For example, **3**)
9. Again, touch in the Command field to activate the touch screen keyboard.
10. Type the **slot** number from step 7 above and press **Enter**. (For example, **3** then press **Enter**.)
11. You should see a command prompt of **#p2c-scope>**
12. Touch in the **Command** field to activate the touch screen keyboard.
13. Type the command **`wb1 350 18 0`** and then press **Enter**. (After the letters wb, the other visible characters are digits. Be sure to type the 3 spaces where shown.)
14. Verify that **`wb1 350 18 0`** is echoed in the console window.
15. You may **Disconnect** and close the **Command Console**.

5.1.3 Difficulty connecting via Ethernet.

Under some conditions, the 980B and 980R Advanced Test Platforms may exhibit difficulty in establishing an Ethernet connection. In this case, if a connection cannot be established after following the Quick Start Guide and common procedures for establishing a network connection, please follow this procedure:

1. Press the front button of the 980 ATP and select Shutdown.
2. After shutdown is complete, turn off the physical power switch beside the mains power cord inlet.

3. While the power switch is OFF, press the front button and hold for a few seconds. Repeat this a few times to assure that all motherboard and power supply capacitors are drained.
4. Make sure the Ethernet connector is connected to your network or PC before powering on the 980 ATP. On Gigabyte motherboards with 2 Ethernet connectors, use the bottom Ethernet connector on 980B, or on the 980R, the Ethernet connecter nearest the mains power inlet.
5. Power on the 980 ATP and allow it to fully boot.
6. Use the normal procedure to establish Ethernet TCP/IP connection with the External 980 Manager software.

5.1.4 HDMI 2.1 Analyzer

There is currently no real-time video display on the HDMI 2.1 Analyzer. This will be added in a future release. Please use Capture Mode Analysis.

5.1.5 HDMI HDCP 2.3 Receiver Compliance Test 2C-01

(2840) When performing test 2C-01 using the HDMI 2.0 Rx/Tx Analyzer module, the test may intermittently fail to display the encrypted video. We expect this to be corrected in the near future. Workarounds:

1. Perform the test multiple times. It may require several passes through the test for the video to display properly.
2. If the 95-00083 HDMI 1.4 Analyzer module is available in the 980, use that module to perform this test.

5.1.6 ARC/SPDIF Analyzer reports IEC headers with all zeros

The ARC/SPDIF Analyzer on the HDMI 1.4 Analyzer module 95-00083 shows IEC headers with all zeros. We expect to correct this in a future release. (2536)

5.1.7 DisplayPort 1.4 Video Generators sometimes produce an extra line of blanking when using formats with very large horizontal active and total

Some video formats with large horizontal active and horizontal total values result in output with an extra vertical blanking line. We expect to correct this in a future release. (2784)

5.1.8 HDMI 2.0 Rx/Tx Analyzer sometimes cannot lock on looped-back playback

When looping back video playback, occasionally the analyzer is unable to lock to the played back TMDS. We expect to correct this in a future release. (2840)

5.1.9 HDMI 2.1 FRL Sink Compliance Test results do not include SCDC in ACA traces

When performing FRL Compliance Tests on a sink device, the saved ACA traces do not include SCDC transactions. We expect to correct this in a future release. (2853)

5.1.10 DP Compliance Test saved test logs always indicate "Passed."

The saved test logs for DisplayPort compliance tests always show the state as passed. (The actual test report does show the correct Pass/Fail state.) We expect to correct this in the next release. (2864)

5.1.11 HDMI 2.1 Video Generator errata

Please note the following limitations with the HDMI 2.1 FRL/TMDS Video Generator in this release. We expect that a future release will overcome these limitations.

- LPCM audio is currently limited to 2 or 8 channels
- High bitrate audio (Dolby TrueHD and DTS Master Audio) is not supported currently.
- VIC2 480p60 YCbCr 4:4:4 8 bpc FRL 3 Gbps 3 lanes fails testing
- VIC2 480p60 RGB 8 bpc FRL 3 Gbps 3 lanes fails testing
- VIC16 1080p60 RGB 8 bpc FRL 6 Gbps 3 lanes fails testing
- VIC16 1080p60 YCbCr 4:4:4 8 bpc FRL 6 Gbps 3 lanes fails testing
- VIC16 1080p60 YCbCr 4:4:4 10 bpc FRL 6 Gbps 3 lanes fails testing
- VIC16 1080p60 RGB 10 bpc FRL 6 Gbps 3 lanes fails testing
- VIC117 2160p100 YCbCr 4:4:4 8 bpc FRL 6 Gbps 4 lanes fails testing
- VIC117 2160p100 RGB 8 bpc FRL 6 Gbps 4 lanes fails testing
- VIC219 4096x2160p120rb YCbCr 4:2:0 10 bpc FRL 6 Gbps 4 lanes can't generate
- VIC118 2160p120rb YCbCr 4:4:4 8 bpc FRL 8 Gbps 4 lanes can't generate
- VIC193 5120x2160p120 YCbCr 4:4:4 8bpc FRL 10 Gbps 4 lanes can't generate
- VIC219 4096x2160p120 YCbCr 4:4:4 10 bpc FRL 10 Gbps 4 lanes can't generate

5.1.12 DP Compliance Test 4.4.4.5 fails with 8 channel audio.

This issue has been corrected and is in testing for the next release. (3107)

5.1.13 DP Compliance Test results in software failure when testing with 8k format 7680x4320p60.

We expect that this issue will be corrected for the next release. (3105)

6 Support

For support on the quantumdata 980 or other Teledyne LeCroy PSG products, please send an email to: psgsupport@teledynelecroy.com

Please include your full contact information and a detailed description of the problem, including product model number, serial number, firmware version, software version, etc.

Appendix A. Compliance Test Reference

A1. DisplayPort Display Stream Compression Compliance Tests: Source Devices

DisplayPort 1.4 Display Stream Compression (DSC) Source Compliance Tests

SKU: 95-00189, License
Required Hardware Module: 95-00151 or 95-00184 or 95-00185
Prerequisite: 95-00155 or 95-00132 DP Analyzer Options, License
Prerequisite: 95-00163 DP 1.4 DSC Analysis, License

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		Available
4.6	**DSC Source Tests**	
4.6.1		
4.6.1.1	DSC enable sequence verifidation	✔
4.6.1.2	DSC PPS block prediction flag verification	✔
4.6.1.3	DSC PPS convert RGB flag verification	✔
4.6.1.4	DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification	✔
4.6.1.5	DSC PPS Simple 4:2:2 flag verification	✔
4.6.1.6	DSC PPS Native 4:2:2 flag verification	✔
4.6.1.7	DSC PPS Native 4:2:0 flag verification	✔
4.5	**Source Device FEC Tests**	
4.5.1	**Source FEC Protocol**	
4.5.1.1	FEC Enable Verification for All Supported Lane Count and Link Speed	✔
4.5.1.2	FEC Ready Verification for Non-FEC Capable Sink	✔

A2. DisplayPort Display Stream Compression Compliance Tests: Sink Devices

DisplayPort 1.4 Display Stream Compression (DSC) Sink Compliance Tests

SKU: 95-00190, License
Required Hardware Module: 95-00151 or 95-00184 or 95-00185
Prerequisite: 95-00154 DP Generator Option, License
Prerequisite: 95-00179 DP 1.4 DSC Transmit, License

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		Available
5.6	**DSC Source Tests**	
5.6.1		
5.6.1.1	DSC capability verification	✔
5.6.1.2	DSC RGB color depth test	✔
5.6.1.3	DSC RGB Block prediction test	✔
5.6.1.4	DSC RGB bits-per-pixel test	✔
5.6.1.5	DSC RGB slice test	✔
5.6.1.6	DSC RGB lanes test	✔
5.6.1.7	DSC YCbCr 4:4:4 color depth test	✔
5.6.1.8	DSC YCbCr 4:4:4 Block prediction test	✔
5.6.1.9	DSC YCbCr 4:4:4 bits-per-pixel test	✔
5.6.1.10	DSC YCbCr 4:4:4 slice test	✔
5.6.1.11	DSC YCbCr 4:4:4 lanes test	✔
5.6.1.12	DSC Simple 4:2:2 color depth test	✔
5.6.1.13	DSC Simple 4:2:2 Block prediction test	✔
5.6.1.14	DSC Simple 4:2:2 bits-per-pixel test	✔
5.6.1.15	DSC Simple 4:2:2 slice test	✔
5.6.1.16	DSC Simple 4:2:2 lanes test	✔
5.6.1.17	DSC Native 4:2:2 color depth test	✔
5.6.1.18	DSC Native 4:2:2 Block prediction test	✔
5.6.1.19	DSC Native 4:2:2 bits-per-pixel test	✔
5.6.1.20	DSC Native 4:2:2 slice test	✔
5.6.1.21	DSC Native 4:2:2 lanes test	✔
5.6.1.22	DSC Native 4:2:0 color depth test	✔
5.6.1.23	DSC Native 4:2:0 Block prediction test	✔
5.6.1.24	DSC Native 4:2:0 bits-per-pixel test	✔
5.6.1.25	DSC Native 4:2:0 slice test	✔
5.6.1.26	DSC Native 4:2:0 lanes test	✔
5.5	**Sink Device FEC Tests**	
5.5.1	**Sink FEC Protocol**	
5.5.1.1	Sink Device FEC Capability Verification	✔
5.5.1.2	Successful Link Training at All Supported Lane Counts and Link Rates with FEC Enable	✔
5.5.1.3	Uncorrectable Block Error Count	✔
5.5.1.4	Correctable Block Error Count	✔
5.5.1.5	Correctable Bit Error Count	✔
5.5.1.6	Correctable Parity Block Error Count	✔
5.5.1.7	Correctable Parity Bit Error Count	✔

A3. DisplayPort Link Layer Compliance Tests: Source Devices

DisplayPort 1.4 Source Protocol Compliance Tests

SKU: 95-00150, License
Required Hardware Module: 95-00151 or 95-00184 or 95-00185
Prerequisite: 95-001 DP 1.4 Analyzer Option, License

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		Available
4.2	**Source Device Services Tests**	
4.2.1	**AUX Reads after Hot Plug Event**	
4.2.1.1	Source DUT Retry on No-Reply during AUX Read After HPD Plug Event	✔
4.2.1.2	Source Retry on Invalid Reply during AUX Read after HPD Plug Event	✔
4.2.1.3	Source Device HPD Event Pulse Length Test	✔
4.2.1.4	Source Device IRQ_HPD Pulse Length Test	✔
4.2.1.5	Source Device Inactive HPD/Inactive AUX Test	✔
4.2.2	**DPCD, DisplayID, and Legacy EDID Reads**	
4.2.2.1	DPCD Receiver Capability Field and EDID Read upon HPD Plug Event	✔
4.2.2.2	DPCD Extended Receiver Capability and EDID Read upon HPD Plug Event	✔
4.2.2.3	EDID Read	✔
4.2.2.4	EDID Read Failure #1: I2C-over-AUX NACK	✔
4.2.2.5	EDID Read Failure #2: I2C-over-AUX DEFER	✔
4.2.2.6	EDID Corruption Detection	✔
4.2.2.7	Branch Device Detection upon HPD Plug Event	✔
4.2.2.8	EDID Read on IRQ_HPD Event after Branch Device Detection	✔
4.2.2.9	E-DDC Four Block EDID Read	✔
4.2.2.10	Link Status/Adjust Request AUX Read Interval during Link Training	✔
4.3	**Source Device Link Services Tests**	
4.3.1	**Link Training**	
4.3.1.1	Successful Link Training at All Supported Lane Counts and Link Speeds	✔
4.3.1.2	Successful Link Training upon HPD Plug Event	✔
4.3.1.3	Successful Link Training with Request of Higher Diff Voltage Swing during Clk Recovery Seq	✔
4.3.1.4	Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing	✔
4.3.1.5	Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing	✔
4.3.1.6	Successful Link Training with Request of a Higher Pre-emphasis during Channel EQ Seq	✔
4.3.1.7	Successful Link Training at Lower Rate Due to Loss of Symbol Lock during Channel EQ Seq	✔
4.3.1.8	Unsuccessful Link Training at Lower Link Rate #1: Iterate at Maximum Voltage Swing	✔
4.3.1.9	Unsuccessful Link Training at Lower Link Rate #2: Iterate at Minimum Voltage Swing	✔
4.3.1.10	Unsuccessful Link Training due to Failure in Channel EQ Sequence (Loop Count > 5)	✔
4.3.1.11	Successful Link Training with Request for Swing and Pre-emphasis during Clk Recovery Seq	✔
4.3.1.12	Source Device Link Training CR Fallback Test	✔
4.3.1.13	Source Device Link Training EQ Fallback Test	✔
4.3.2	**Link Maintenance**	
4.3.2.1	Successful Link Retraining after IRQ_HPD Pulse Due to Loss of Symbol Lock	✔
4.3.2.2	Successful Link Retraining after IRQ_HPD Pulse Due to Loss of Clock Recovery Lock	✔
4.3.2.3	Successful Link Retraining after IRQ_HPD Pulse Due to Loss of Inter-lane Alignment Lock	✔
4.3.2.4	Handling of IRQ_HPD Pulse with No Error Status Bits Set	✔
4.3.2.5	Lane Count Reduction (Deprecated)	✔
4.3.3	**Video Time Stamp Generation**	
4.3.3.1	Video Time Stamp Generation	✔
4.4	**Source Device Isochronous Transport Services Tests**	
4.4.1	**Main Stream Data Mapping**	
4.4.1.1	Pixel Data Packing and Steering	✔
4.4.1.2	Main Stream Data Packing and Stuffing – Least-packed TU	✔
4.4.1.3	Main Stream Data Packing and Stuffing – Most-packed TU	✔
4.4.2	**Main Video Stream Format Change Handling**	
4.4.2.1	Main Video Stream Format Change Handling	✔
4.4.3	**Power Management**	
4.4.3.1	Power Management	✔
4.4.4	**Audio Stream Transmission over Secondary Packets**	
4.4.4.1	Configuring Video and Audio Parameters	
4.4.4.2	Audio Stream Header Synchronization	✔
4.4.4.3	Audio Time Stamp Generation	✔
4.4.4.4	Audio INFOFRAME Packet	✔
4.4.4.5	Audio Stream Transmission	✔
4.4.4.6	Audio Start Sequence	✔
4.5	**Source Device FEC Tests**	
4.5.1	**Source FEC Protocol**	
4.5.1.1	FEC Enable Verification for All Supported Lane Count and Link Speed	✔
4.5.1.2	FEC Ready Verification for Non-FEC Capable Sink	✔

A4. DisplayPort Link Layer Compliance Tests: Sink Devices

DisplayPort 1.4 Sink Protocol Compliance Tests

SKU: 95-00170, License
Required Hardware Module: 95-00151 or 95-00184 or 95-00185
Prerequisite: 95-001 DP 1.4 Analyzer Option, License

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		Available
5.2	**Sink Device Services Tests**	
5.2.1	**AUX_CH Protocol**	
5.2.1.1	Read One Byte from Valid DPCD Address	✔
5.2.1.2	DPCD Receiver Capability Read	✔
5.2.1.3	Write One Byte to Valid DPCD Address	✔
5.2.1.4	Write Nine Bytes to Valid DPCD Addresses	✔
5.2.1.5	Write EDID Offset	✔
5.2.1.6	Read One EDID Byte	✔
5.2.1.7	EDID Read	✔
5.2.1.8	Illegal AUX Request Syntax	✔
5.2.1.9	Glitch Rejection	✔
5.2.1.10	Interleaved EDID and DPCD Receiver Capability Read	✔
5.2.1.11	Downstream Stop on MOT Reset	✔
5.2.1.12	Downstream Stop on Timeout	✔
5.2.2	**Sink Device DPCD Field Implementation**	
5.2.2.1	Sink Organizationally Unique Identifier	✔
5.2.2.2	Sink Count	✔
5.2.2.3	Sink Status	✔
5.2.2.4	Sink Error Count	✔
5.2.2.5	DPCD Address Range	✔
5.2.2.6	Number of Receiver Ports	✔
5.2.2.7	Main-Link Channel Coding	✔
5.2.2.8	ESI Field Mapping	✔
5.2.2.9	Sink Device Symbol Error Count	✔
5.3	**Sink Device Link Services Tests**	
5.3.1	**Link Training**	
5.3.1.1	Successful Link Training at All Supported Lane Counts and Link Speeds	✔
5.3.1.2	Successful Link Training with Request of Higher Diff Swing during Clock Recovery Seq	✔
5.3.1.3	Successful Link Training to a Lower Link Rate Due to Clk Rcvy Lk Fail during Clk Rcvy Seq	✔
5.3.1.4	Successful Link Training with Req of Chg to Pre-Emph and/or Swing during Chan EQ Seq	✔
5.3.1.5	Successful Link Training at Lower Link Rate Due to Loss of Sym Lk during Link Training Seq	✔
5.3.1.6	Lane Count Reduction	✔
5.3.1.7	Lane Count Increase	✔
5.3.1.8	2-Lane Link Training CR/EQ Fallback Test	✔
5.3.1.9	1-Lane Link Training CR/EQ Fallback Test	✔
5.3.2	**Link Maintenance**	
5.3.2.1	IRQ_HPD Pulse Due to Loss of Symbol Lock and Clock Recovery	✔
5.3.2.2	IRQ_HPD Pulse Due to Inter-lane Alignment Loss	✔
5.4	**Sink Device Isochronous Transport Services Tests**	
5.4.1	**Main Video Stream Reproduction**	
5.4.1.1	Pixel Data Reconstruction	✔
5.4.1.2	Main Stream Data Unpacking and Unstuffing – Least-packed TU	✔
5.4.1.3	Main Stream Data Unpacking and Unstuffing – Most-packed TU	✔
5.4.1.4	Pixel Clock Recovery	✔
5.4.2	**Main Video Stream Format Change Handling**	
5.4.2	Main Video Stream Format Change Handling	✔
5.4.3	**Power Mangement**	
5.4.3.1	Entering and Exiting Power Save Mode	✔
5.4.3.2	Resumption of Main-Link Activity after Extended Idle	✔
5.4.4	**Main Audio Stream Reconstruction**	
5.4.4.1	Audio Test Patterns	✔
5.4.4.2	Audio Startup and Format Change	✔
5.4.4.3	RS Error Correction	✔
5.4.4.4	Audio Infoframe Packet	✔
5.4.4.5	Audio Clock Recovery	✔
5.4.4.6	Audio Stream Reception	✔
5.5	**Sink Device FEC Tests**	
5.5.1	**Sink FEC Protocol**	
5.5.1.1	Sink Device FEC Capability Verification	✔
5.5.1.2	Successful Link Training at All Supported Lane Counts and Link Rates with FEC Enable	✔
5.5.1.3	Uncorrectable Block Error Count	✔
5.5.1.4	Correctable Block Error Count	✔
5.5.1.5	Correctable Bit Error Count	✔
5.5.1.6	Correctable Parity Block Error Count	✔
5.5.1.7	Correctable Parity Bit Error Count	✔

A5. HDMI 2.1 FRL Compliance Tests: Source Devices

HDMI 2.1 Source FRL Protocol Compliance Tests

SKU: 95-00174, License 66
Required Hardware Module: 95-00156
Prerequisite: 95-00157 HDMI 2.1 Analyzer Software, License 53
(HFR1-66 currently requires 95-00137)

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		Available
4.2.2	**Source FRL Protocol Tests**	
4.2.2.1	**Source Low-Level FRL Protocol Tests**	
HFR1-11	: Source FRL Protocol – Legal Codes	✔
HFR1-19	: Source FRL Packets – FRL Map Characters	✔
HFR1-20	: Source FRL Packets – FRL Control Periods	✔
HFR1-21	: Source FRL Packets – Active Video FRL Packets (Uncompressed)	✔
HFR1-22	: Source FRL Packets – Active Video FRL Packets (Compressed)	
HFR1-23	: Source FRL Protocol – Data Flow Metering Variations	✔
4.2.2.2	**Source FRL Link Training Tests**	
HFR1-10	: Source FRL Protocol – FRL Link Training Patterns	
HFR1-12	: Source FRL Protocol – Successful FRL Link Training	✔
HFR1-13	: Source FRL Protocol –FRL Link Training – Link Rate Change	✔
HFR1-17	: Source FRL Protocol –FRL Link Training – Future Rate Support	✔
4.2.3	**Source FRL Pixel Encoding Tests**	
4.2.3.1	**Source 8 bpc Pixel Encoding Tests**	
HFR1-29	: Source Pixel Encoding (FRL Mode) – RGB	✔
HFR1-30	: Source Pixel Encoding (FRL Mode) – YCBCR 4:2:2/4:4:4	✔
HFR1-31	: Source Pixel Encoding (FRL Mode) – YCBCR 4:2:0	✔
4.2.3.2	**Source Deep Color Pixel Encoding Tests**	
HFR1-27	: Source Pixel Encoding (FRL Mode) – Non-YCBCR 4:2:0 Deep Color	✔
HFR1-32	: Source Pixel Encoding (FRL Mode) – YCBCR 4:2:0 Deep Color	✔
4.2.4	**Source Video Timing Tests**	
4.2.4.1	**Source 8bpc Video Timing Tests**	
HFR1-14	: Source Video Timing (FRL Mode) – Sub-2160p 24-bit Color Depth	✔
HFR1-24	: Source Video Timing (FRL Mode) – 2160p 24-bit Color Depth	✔
HFR1-33	: Source Video Timing (FRL Mode) – YCBCR 4:2:0	✔
HFR1-50	: Source Video Timing (FRL Mode) – 4320p 24-bit Color Depth	✔
4.2.4.2	**Source Deep Color Video Timing Tests**	
HFR1-15	: Source Video Timing (FRL Mode) – Sub-2160p Deep Color	✔
HFR1-25	: Source Video Timing (FRL Mode) – 2160p Deep Color	✔
HFR1-34	: Source Video Timing (FRL Mode) – YCBCR 4:2:0 Deep Color	✔
HFR1-35	: Source Video Timing (FRL Mode) – 4320p Deep Color	✔
4.2.4.3	**Source 3D Video Timing Tests**	
HFR1-16	: Source Video Timing (FRL Mode) – 2160p 3D	✔
HFR1-26	: Source Video Timing (FRL Mode) – Non-2160p 3D	✔
4.2.4.4	**Source Marketing Feature Names Tests**	
HFR1-MFN	: Source Video Timing (FRL Mode) – Marketing Feature Names	✔
4.2.5	**Source FRL Audio Encoding Tests**	
4.2.5.1	**Source Basic Audio Tests**	
HFR1-45	: Source Audio Channel Status (FRL Mode) – Basic Audio – Allowed Rate	✔
HFR1-46	: Source Audio Encoding (FRL Mode) – Audio Clock Generation	✔
4.2.5.2	**Source Compressed Audio Tests**	
HFR1-40	: Source Audio Encoding (FRL Mode) – CTA-861-G Audio	✔
HFR1-43	: Source Audio Encoding (FRL Mode) – HBR Audio – IEC Audio Stream Packet	✔
4.2.5.3	**Source One Bit Audio Tests**	
4.2.5.4	**Source 3D Audio Tests**	
HFR1-36	: Source Audio Encoding (FRL Mode) – 3D Audio (L-PCM) – Packet Format	✔
HFR1-37	: Source Audio Encoding (FRL Mode) – 3D Audio (One Bit) – Packet Format	✔
HFR1-41	: Source Audio Encoding FRL Mode 3D Audio – IEC Sample Packet	✔
4.2.5.5	**Source Multi-stream Audio Tests**	
HFR1-38	: Source Audio Encoding (FRL Mode) – MS Audio (L-PCM and 61937) – Packet Format	✔
HFR1-39	: Source Audio Encoding (FRL Mode) – MS Audio (One Bit) – Packet Format	✔
HFR1-42	: Source Audio Encoding (FRL Mode) – MS Audio – IEC Sample Packet	
4.2.6	**Source FRL HDMI-VSIFs Tests**	
HFR1-47	: Source HDMI-VSIFs (FRL Mode) – 3D OSD Disparity	
HFR1-48	: Source HDMI-VSIFs (FRL Mode) – Dual-View	
HFR1-49	: Source HDMI-VSIFs (FRL Mode) – Independent-View	
4.2.7	**Source FRL AVI InfoFrame and GCP Tests**	
4.2.7.1	**Source AVI InfoFrame and GCP Tests**	
HFR1-18	: Source AVI InfoFrame and GCP (FRL Mode) – Legacy 2160p	✔
HFR1-28	: Source AVI InfoFrame and GCP (FRL Mode) – Legacy Non-2160p	✔
4.2.7.2	**Source AVI InfoFrame for Y420VDB and Y420CMDB Tests**	
HFR1-51	: Source AVI InfoFrame for Y420VDB and Y420CMDB (FRL Mode)	✔
4.2.7.3	**Source AVI InfoFrame and GCP BT.2020 Tests**	
HFR1-52	: Source AVI InfoFrame and GCP (FRL Mode) - YCBCR 4:2:0 BT.2020	✔
4.2.8	**Source FRL Audio InfoFrame Tests**	
HFR1-44	: Source Audio InfoFrame (FRL Mode) – 3D and MS Audio (One Bit) – Supported Frequency	✔
4.2.9	**Source FRL High Dynamic Range Tests**	
4.2.10	**Source FRL Extended Metadata Packet (EMP) Tests**	
HFR1-65	: Transport of Compressed Video Transport Extended Metadata (CVTEM)	
4.2.11	**Source E-EDID Tests**	
HFR1-66	: Source EDID Reading – VESA E-EDID 1.3	✔

A6. HDMI 2.1 FRL Compliance Tests: Sink Devices

HDMI 2.1 Sink FRL Compliance Tests

SKU: 95-00175, License 67
Required Hardware Module: 95-00156
Prerequisite: 95-00158 HDMI 2.1 Generator, License 52

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		Available
4.2.2	**Sink FRL Protocol Tests**	
4.2.2.1	**Sink Character Error Detection Tests**	
HFR2-17	: Sink FRL Protocol – CED – Lock Bits	✔
HFR2-18	: Sink FRL Protocol – CED – Error Counting During Reads	✔
HFR2-19	: Sink FRL Protocol – CED – Specific Video Data Error Injection	✔
HFR2-20	: Sink FRL Protocol – CED – Maximum Video Data Error Injection	✔
HFR2-21	: Sink FRL Protocol – CED – Update Flag with Specific Error Injection	✔
HFR2-22	: Sink FRL Protocol – CED – Update Flag with Maximum Error Injection	✔
4.2.2.2	**Sink Error Correction Tests**	
HFR2-48	: Sink FRL Protocol – RS – Basic Operation	✔
HFR2-49	: Sink FRL Protocol – RS – Correction Counting During Reads	✔
HFR2-50	: Sink FRL Protocol – RS – Maximum Symbol Error Count	✔
HFR2-51	: Sink FRL Protocol – RS – Update Flag with Specific Symbol Error Count	✔
HFR2-52	: Sink FRL Protocol – RS – Update Flag with Maximum Symbol Error Count	✔
4.2.3	**Sink FRL Pixel Decoding Tests**	
4.2.3.1	**Sink 8 bpc Pixel Decoding Tests**	
HFR2-31	: Sink Pixel Decoding (FRL Mode) – RGB	✔
HFR2-32	: Sink Pixel Decoding (FRL Mode) – YCBCR 4:2:2/4:4:4	✔
HFR2-23	: Sink Pixel Decoding (FRL Mode) – YCBCR 4:2:0	✔
4.2.3.2	**Sink 8 bpc Pixel Decoding Tests**	
HFR2-24	: Sink Pixel Decoding (FRL Mode) – YCBCR 4:2:0 Deep Color	✔
HFR2-33	: Sink Pixel Decoding (FRL Mode) – Non-YCBCR 4:2:0 Deep Color	✔
4.2.4	**Sink FRL Video Timing Tests**	
4.2.4.1	**Sink 8 bpc Video Timing Tests**	
HFR2-11	: Sink Video Timing (FRL Mode) – Sub-2160p 24-bit Color Depth	✔
HFR2-12	: Sink Video Timing (FRL Mode) – 2160p 24-bit Color Depth	✔
HFR2-13	: Source Video Timing (FRL Mode) – 4320p 24-bit Color Depth	✔
4.2.4.2	**Sink Deep Color Video Timing Tests**	
HFR2-14	: Sink Video Timing (FRL Mode) – Sub-2160p Deep Color	✔
HFR2-15	: Sink Video Timing (FRL Mode) – 2160p Deep Color	✔
HFR2-16	: Sink Video Timing (FRL Mode) – 4320p Deep Color	✔
4.2.4.3	**Source 3D Video Timing Tests**	
4.2.5	**Sink FRL Audio Decoding and Rendering Tests**	
4.2.5.1	**Sink Basic Audio Tests**	
4.2.5.2	**Sink Compressed Audio Tests**	
HFR2-27	: Sink Audio Decoding and Rendering (FRL Mode) – CTA-861-G Audio	
4.2.5.3	**Sink One Bit Audio Tests**	
4.2.5.4	**Sink 3D Audio Tests**	
HFR2-28	: Sink Audio Decoding and Rendering (FRL Mode) – 3D Audio (L-PCM) – Sample Packet	
HFR2-29	: Sink Audio Decoding and Rendering (FRL Mode) – 3D Audio (One Bit) – Sample Packet	
4.2.5.5	**Sink Multi-stream Audio Tests**	
HFR2-30	: Sink Audio Decoding and Rendering (FRL) – Multi-stream (L-PCM and 61937) – Sample Packe	✔
HFR2-46	: Sink Audio Decoding and Rendering (FRL Mode) – Multi-Stream (One Bit) – Sample Packet	
4.2.6	**Sink FRL A/V Relationship Tests**	
HFR2-42	: Sink A/V Relationship (FRL Mode) – Dynamic Auto Lipsync (DALS)	
4.2.7	**Sink FRL HDMI-VSIF Tests**	
HFR2-40	: Sink HDMI-VSIFs (FRL Mode) – Dual-View	✔
HFR2-43	: Sink HDMI-VSIFs (FRL Mode) – 3D OSD Disparity	✔
4.2.8	**Sink FRL E-EDID Tests**	
HFR2-53	: Sink Video Timing – FRL/Gaming/DSC – HF-VSDB	✔
HFR2-70	: Sink EDID - HF-VSDB Reserved Bits	✔
4.2.9	**Sink FRL Extended Metadata Packet (EMP) Tests**	

A7. HDMI 2.1 eARC Compliance Tests: eARC Tx Devices

HDMI 2.1 eArc TX Compliance Tests

SKU: 95-00167, License 59
Required Hardware Module: 95-00156
Prerequisite: 95-00165 Functional Test of eARC TX, License 57

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		Available
6.1.2	**eARC TX Common Mode Protocol Tests**	
6.1.2.1	**eARC TX Common Mode Regular Tests**	
HFR5-1-20	: eARC TX eARC Discovery With COMMA Width Margining	✔
HFR5-1-21	: eARC TX Command Behavior With Bit Time Margining	✔
HFR5-1-22	: eARC TX gets <NACK> indicating eARC RX Busy	✔
HFR5-1-23	: eARC TX gets Common Mode Slow Response	✔
6.1.2.2	**eARC TX Common Mode Irregular Behavior Tests**	
HFR5-1-24	: eARC TX gets Timeout during Heartbeat	✔
HFR5-1-25	: eARC TX gets Heartbeat Disconnect	✔
HFR5-1-26	: eARC TX gets HPD LOW Disconnect	✔
HFR5-1-50	: eARC TX Responds <RETRY> to Read Data Packet With Uncorrectable ECC Error	✔
HFR5-1-55	: eARC TX gets Heartbeat Failure during Discovery	✔
6.1.3	**eARC TX Audio Protocol Tests**	
6.1.3.1	**eARC TX LPCM Protocol Tests**	
HFR5-1-28	: eARC TX 2-channel LPCM Audio Packet Structure	✔
HFR5-1-29	: eARC TX Multi-Channel 2-channel layout LPCM Audio Packet Structure	✔
HFR5-1-56	: eARC TX Multi-Channel 8-channel layout LPCM Audio Packet Structure	✔
HFR5-1-58	: eARC TX Multi-Channel 16-channel layout LPCM Audio Packet Structure	✔
HFR5-1-59	: eARC TX Multi-Channel 32-channel layout LPCM Audio Packet Structure	✔
6.1.3.2	**eARC TX Compressed Audio Protocol Tests**	
HFR5-1-27	: eARC TX Compressed Layout A Audio Packet Structure	✔
HFR5-1-40	: eARC TX Compressed Layout B Audio Packet Structure	✔
6.1.3.3	**eARC TX Format Change Tests**	
HFR5-1-30	: eARC TX Behavior on Audio Format Change	✔
6.1.4	**eARC TX Audio Rate and Content Tests**	
6.1.4.1	**eARC TX LPCM Rate and Content Tests**	
HFR5-1-32	: eARC TX 2-channel LPCM Audio Rates	✔
HFR5-1-33	: eARC TX Multi-channel 2-channel layout LPCM Audio Rates	✔
HFR5-1-34	: eARC TX LPCM Channel Allocation Field	✔
HFR5-1-57	: eARC TX Multi-channel 8-channel layout LPCM Audio Rates	✔
HFR5-1-60	: eARC TX Multi-channel 16-channel layout LPCM Audio Rates	✔
HFR5-1-61	: eARC TX Multi-channel 32-channel layout LPCM Audio Rates	✔
6.1.4.2	**eARC TX Compressed Audio Rate Tests**	
HFR5-1-31	: eARC TX Compressed Layout A Audio Rates	✔
HFR5-1-41	: eARC TX Compressed Layout B Audio Rates	✔
6.1.5	**eARC TX Capabilities Data Structure and Status Data Tests**	
HFR5-1-35	: eARC TX Reads Capabilities Data Structure at startup	✔
HFR5-1-36	: eARC TX Re-reads Capabilities Data Structure when CAP_CHNG->1	✔
6.1.6	**eARC TX Audio Lip-sync Tests**	
HFR5-1-37	: eARC TX Re-reads ERX_LATENCY when STAT_CHNG->1	✔
6.1.7	**eARC TX HPD and HDMI_HPD Tests**	
HFR5-1-38	: eARC TX set HPD LOW when leaving Standby Test	✔
HFR5-1-39	: eARC TX EDID Update and HDMI_HPD Test	✔
HFR5-1-51	: eARC TX EDID Update and HPD on CDS Change Test	✔
6.1.8	**eARC TX eARC Audio Source Tests**	
HFR5-1-62	: eARC TX Sends Audio from all Sources over eARC	✔
6.1.9	**eARC TX ARC Tests**	
HFR5-1-52	: eARC TX eARC Discovery Fails, Try ARC Fallback	✔

A8. HDMI 2.1 eARC Compliance Tests: eARC Rx Devices

HDMI 2.1 eArc RX Compliance Tests

SKU: 95-00168, License 60
Required Hardware Module: 95-00156
Prerequisite: 95-00166 Functional Test of eARC TX, License 58

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		Available
6.1.2	**eARC RX Common Mode Protocol Tests**	
6.1.2.1	**eARC RX Common Mode Regular Tests**	
HFR5-2-20	: eARC RX eARC Discovery With COMMA Response Margining	✔
HFR5-2-21	: eARC RX Command Behavior With Bit Time Margining	✔
HFR5-2-22	: eARC RX Behavior if no response to eARC Discovery	✔
6.1.2.2	**eARC RX Common Mode Irregular Behavior Tests**	
HFR5-2-23	: eARC RX gets Unexpected Device ID	✔
HFR5-2-24	: eARC RX gets new Opcode in the middle of a Command	✔
HFR5-2-25	: eARC RX gets Heartbeat Disconnect	✔
HFR5-2-26	: eARC RX gets HPD LOW during eARC Discovery	✔
HFR5-2-27	: eARC RX gets HPD LOW after eARC established	✔
HFR5-2-53	: eARC RX Receives <RETRY> indicating eARC TX Error Detection	✔
6.1.3	**eARC RX Audio Protocol Tests**	
6.1.3.1	**eARC RX LPCM Protocol Tests**	
HFR5-2-29	: eARC RX 2-channel layout LPCM Audio Mute	✔
HFR5-2-30	: eARC RX Multi-channel 8-channel layout LPCM Audio Mute	✔
HFR5-2-54	: eARC RX Multi-channel 16-channel layout LPCM Audio Mute	✔
HFR5-2-55	: eARC RX Multi-channel 32-channel layout LPCM Audio Mute	✔
6.1.3.2	**eARC RX Compressed Audio Protocol Tests**	
HFR5-2-28	: eARC RX Compressed Layout A Audio Mute	✔
HFR5-2-31	: eARC RX Compressed Audio Layout A Error Correction	✔
HFR5-2-40	: eARC RX Compressed Layout B Audio Mute	✔
HFR5-2-52	: eARC RX Compressed Audio Layout B Error Correction	✔
6.1.4	**eARC RX Audio Rate and Content Tests**	
6.1.4.1	**eARC RX LPCM Rate and Content Tests**	
HFR5-2-33	: eARC RX Multi-channel 2-channel layout LPCM Audio Rates	✔
HFR5-2-34	: eARC RX Multi-channel 8-channel layout LPCM Audio Rates	✔
HFR5-2-35	: eARC RX LPCM Channel Allocation Field	✔
HFR5-2-56	: eARC RX Multi-channel 16-channel layout LPCM Audio Rates	✔
6.1.4.2	eARC RX Compressed Audio Rate Tests	
HFR5-2-32	: eARC RX Compressed Layout A Audio Rates	✔
HFR5-2-41	: eARC RX Compressed Layout B Audio Rates	✔
6.1.5	**eARC RX Capabilities Data Structure and Status Data Tests**	
HFR5-2-36	: eARC RX Capabilities Data Structure	✔
6.1.6	**eARC RX Audio Lip-sync Tests**	
HFR5-2-37	: eARC RX Announces ERX_LATENCY With STAT_CHNG->1	✔
6.1.7	**eARC RX HDMI_HPD Tests**	
HFR5-2-39	: eARC RX HDMI_HPD and TX EDID Test	✔
6.1.8	**eARC RX ARC Tests**	
HFR5-2-50	: eARC RX eARC Discovery Fails, Try ARC Fallback	✔