Essentials of DisplayPort Protocols at HBR3 Link Rates - 8.1Gbps

Webinar – June – 2017
Agenda

- Aux Channel
  - Link Training at 8.1Gbps Link Rates
  - HDCP 2.2 (not covered in detail)
- Main Link – Video/Audio Stream Transmission
  - Video packets
  - Metadata (Main Stream Attributes)
  - Secondary data packets (Audio)
  - Control symbols
- Q & A
- Brief Survey

Please feel free to contact me, Neal Kendall at: neal.kendall@teledyne.com
If you have any questions.
DisplayPort Anatomy

- Main Link: Unidirectional, high-bandwidth channel used to transport video, audio and metadata and protocol control elements.
- Main Link 1, 2 or 4 Lane Configurations.
- Main Link 4 link rates:
  - 1.62Gbps (Reduced Bit Rate)
  - 2.7Gbps (High Bit Rate)
  - 5.4Gbps (High Bit Rate 2)
  - 8.1Gbps (High Bit Rate 3) introduced in DisplayPort 1.3/4.
- No clock channel. Sink recovers clock using link transitions.
- Aux Channel: Bidirectional, half duplex channel with a data rate of 1Mbps. Link Training, DPCD Register status, HDCP authentication & EDID.
- Hot plug lead:
  - Connection Detection.
  - Interrupt mechanism in cases where there is a failure.
DisplayPort Connection Sequence

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DisplayPort Connection Sequence

- **Hot Plug.** Indication to the Source that there is a Display device connect to it.
- **EDID read.** EDID is a data structure provided by a DisplayPort display that describe its capabilities to a DisplayPort video source.
- **Link Training.** Link training establishes the physical link parameters (number of lanes, link rate, voltage swing, pre-emphasis, equalization) used for transmission of video and audio over the main link.
  - **Link Training** has two phases:
    - Clock Recovery
    - Channel Equalization which includes Symbol Lock and Inter-Lane alignment.
- **If the video/audio content is flagged for content protection,** the High-bandwidth Digital Content Protection (HDCP) authentication protocol is used.

**DisplayPort Source**

**DisplayPort Sink (Monitor/TV)**

- **DisplayPort Cable**
- **Event(s)**

**Hot Plug**

- **Read EDID Capabilities of Sink Device**
- **Read DPCD Link Capabilities of Sink**
- **Link Training – Clock Recovery**
- **Link Training – Channel Equalization, Symbol Lock, Lane Alignment**
- **HDCP Authentication**
  For content protection
DisplayPort Aux Channel Monitoring

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Monitoring the DP Aux Channel – Emulating a DP Source to Test a DP Display

Teledyne LeCroy quantumdata 980 Test Platform with DP 1.4 Video Generator / Protocol Analyzer module emulating DisplayPort Source

DisplayPort Cable

DisplayPort Sink (Monitor/TV)
Monitoring the DP Aux Channel – Emulating a DP Sink to Test a DP Display

Teledyne LeCroy quantumdata 980 Test Platform with DP 1.4 Video Generator / Protocol Analyzer module emulating DisplayPort Sink
Passive Monitoring of Aux Channel Between a DP Sink and Display

Teledyne LeCroy quantumdata 980 Test Platform with DP 1.4 Video Generator / Protocol Analyzer Passively Monitoring DP Aux Channel
Two panels:
1) Transaction Log Panel
2) Details panel.

Details of the highlighted transaction in the Log panel appears in the Details panel.

Time goes from top to bottom on the Transaction Log panel.
980 Auxiliary Channel Analyzer Transactions

- Direction of transaction is provided (< >).
- Read and Write is indicated (R W).
- Message type indicated (e.g. DPLT for DisplayPort Link Training). Color coding also used to distinguish between transaction types.
DisplayPort Connection Sequence Link Training

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Connection Sequence – EDID Read

**DisplayPort Source**
- Source Function
- Read Request for Sink DPCD
- Capabilities over Aux Chan
- Returns DPCD Capability Registers over Aux Chan
- Writes Link Configuration Parameters over Aux Chan
- Transmit Training Pattern 1 symbols over Main Link
- Write current drive settings to Rx DPCD over Aux Chan
- Read Request on DPCD - CR Done over Aux Chan
- If CR not Done, then adjust Voltage Swing and Pre-Emphasis
- Repeat if CR if not done; Otherwise: Channel EQ.

**DisplayPort Sink**
- Sink Function
- Transaction
- Hot Plug
- Send EDID over Aux Chan
- Checks if CR is achieved
- Source Reads EDID from Sink

**Source Reads EDID from Sink**
- EDID
- Returns CR Status from DPCD over Aux Chan
- Transmit Training Pattern 1 symbols over Main Link
- Checks if CR is achieved
- > 100us
- Write current drive settings to Rx DPCD over Aux Chan
- Read Request on DPCD - CR Done over Aux Chan
- Transmit Training Pattern 1 symbols over Main Link
- Checks if CR is achieved
Connection Sequence – Sample EDID Contents

[Images of screenshots showing EDID contents and settings on a computer interface]
Connection Sequence – Read Sink DPCD Capabilities

**DisplayPort Source**

Transaction
- **Hot Plug**
  - Send EDID over Aux Chan

**Source Function**
- Read Request for Sink DPCD Capabilities over Aux Chan
- Returns DPCD Capability Registers over Aux Chan
- Writes Link Configuration Parameters over Aux Chan
- Transmit Training Pattern 1 symbols over Main Link
- Write current drive settings to Rx DPCD over Aux Chan
- Read Request on DPCD - CR Done over Aux Chan
- Returns CR Status from DPCD over Aux Chan
- Transmit Training Pattern 1 symbols over Main Link

*Source selects Voltage Swing and Pre-Emphasis for TPS1*

*If CR not done, then adjust Voltage Swing and Pre-Emphasis*

**DisplayPort Sink**

Transaction
- **Read Request for Sink DPCD Capabilities**
- Returns DPCD Capability Registers over Aux Chan

**Sink Function**
- Checks if CR is achieved
- Transmits Training Pattern 1 symbols over Main Link
- Write current drive settings to Rx DPCD over Aux Chan
- Read Request on DPCD - CR Done over Aux Chan
- Returns CR Status from DPCD over Aux Chan
- Transmit Training Pattern 1 symbols over Main Link

*Repeat if CR if not done; Otherwise: Channel EQ.*
Connection Sequence – Link Training Clock Recovery Sequence

DisplayPort Source
Source Function
Transaction
Source Function
 направлен на Sink
Sink Function
 направлен на Source

Source Writing Link Rate (8.1Gbps) to Sink DPCD Registers to Begin Link Training

- **Source Function**: Transmit Training Pattern 1 symbols over Main Link
- **Sink Function**: Checks if CR is achieved
- **Source Function**: Returns CR Status from DPCD over Aux Chan
- **Sink Function**: Checks if CR is achieved
- **Source Function**: Transmits Link Configuration Parameters over Aux Chan
- **Sink Function**: Checks if CR is achieved
- **Source Function**: Transmit Training Pattern 1 symbols over Main Link
- **Source Function**: Repeat if CR if not done; Otherwise: Channel EQ.
- **Source Function**: Write current drive settings to Rx DPCD over Aux Chan
- **Source Function**: > 100us
- **Source Function**: Read Request on DPCD - CR Done over Aux Chan
- **Source Function**: Returns DPCD Capability Registers over Aux Chan
- **Source Function**: Return Request for Sink DPCD Capabilities over Aux Chan
- **Source Function**: Send EDID over Aux Chan
- **Source Function**: Hot Plug

Source selects Voltage Swing and Pre-Emphasis for TPS1
### Connection Sequence – Link Training Clock Recovery Sequence

<table>
<thead>
<tr>
<th>DisplayPort Source</th>
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<th>DisplayPort Sink</th>
<th>Source Function</th>
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<tbody>
<tr>
<td><strong>Source Function</strong></td>
<td><strong>Transaction</strong></td>
<td><strong>Sink Function</strong></td>
<td><strong>Source Writing Lane Count to Sink</strong></td>
</tr>
<tr>
<td>Source selects Voltage Swing and Pre-Emphasis for TPS1</td>
<td>Send EDID over Aux Chan</td>
<td><strong>Read Request for Sink DPCD Capabilities over Aux Chan</strong></td>
<td>DPCD Registers to Begin Link Training</td>
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<td>Returns DPCD Capability Registers over Aux Chan</td>
<td><strong>Writes Link Configuration Parameters over Aux Chan</strong></td>
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<td>Repeat if CR if not done; Otherwise: Channel EQ.</td>
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</table>

- If CR not done, then adjust Voltage Swing and Pre-Emphasis.
- Source selects Voltage Swing and Pre-Emphasis for TPS1.
- Transmits Training Pattern 1 symbols over Main Link.
- Checks if CR is achieved.

**Source Writing Lane Count to Sink DPCD Registers to Begin Link Training**
Connection Sequence – Link Training Clock Recovery Sequence

- DisplayPort Source
  - Source Function
  - Transaction
    - Hot Plug
      - Send EDID over Aux Chan
  - Read Request for Sink DPCD
    - Capabilities over Aux Chan
    - Returns DPCD Capability Registers over Aux Chan
  - Writes Link Configuration Parameters over Aux Chan
    - Transmit Training Pattern 1 symbols over Main Link
    - Write current drive settings to Rx DPCD over Aux Chan
  - If CR not done, then adjust Voltage Swing and Pre-Emphasis

- DisplayPort Sink
  - Sink Function
  - Transaction
    - Hot Plug
      - Send EDID over Aux Chan
  - Read Request for Sink DPCD
    - Capabilities over Aux Chan
    - Returns DPCD Capability Registers over Aux Chan
  - Checks if CR is achieved
    - Transmit Training Pattern 1 symbols over Main Link
    - Write current drive settings to Rx DPCD over Aux Chan
  - Checks if CR is achieved
    - Read Request on DPCD - CR Done over Aux Chan
    - Returns CR Status from DPCD over Aux Chan
  - If CR not done, then adjust Voltage Swing and Pre-Emphasis
  - Transmit Training Pattern 1 symbols over Main Link

Source writing Downspread control indicating that down spreading is not used.
Connection Sequence – Link Training Clock Recovery Sequence

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<tr>
<td>Transaction</td>
<td>Hot Plug</td>
</tr>
<tr>
<td>Read Request for Sink DPCD</td>
<td>Send EDID over Aux Chan</td>
</tr>
<tr>
<td>Capabilities over Aux Chan</td>
<td>Returns DPCD Capability Registers over Aux Chan</td>
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<tr>
<td>Writes Link Configuration Parameters over Aux Chan</td>
<td>Transmit Training Pattern 1 symbols over Main Link</td>
</tr>
<tr>
<td>Source selects Voltage Swing and Pre-Emphasis for TPS1</td>
<td>Source Writing Training Pattern Set 1 that will be used during Link Training to Sink DPCD Registers</td>
</tr>
<tr>
<td>Transmit Training Pattern 1 symbols over Main Link</td>
<td>Checks if CR is achieved</td>
</tr>
<tr>
<td>Write current drive settings to Rx DPCD over Aux Chan &gt; 100us</td>
<td>Checks if CR is achieved</td>
</tr>
<tr>
<td>Read Request on DPCD - CR Done over Aux Chan</td>
<td>Repeat if CR if not done; Otherwise: Channel EQ.</td>
</tr>
<tr>
<td>Returns CR Status from DPCD over Aux Chan</td>
<td>Repeat if CR if not done; Otherwise: Channel EQ.</td>
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### Connection Sequence – Link Training Clock Recovery Sequence

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<td><strong>Source Function</strong></td>
<td></td>
<td><strong>Source Writing Voltage Swing and Pre-Emphasis Levels that will be used for Link Training to Sink DPCD Registers</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Send EDID over Aux Chan</strong></td>
<td><strong>Read Request for Sink DPCD Capabilities over Aux Chan</strong></td>
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<td><strong>Read Request for Sink DPCD Capabilities over Aux Chan</strong></td>
<td><strong>Returns DPCD Capability Registers over Aux Chan</strong></td>
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<td><strong>Write current drive settings to Rx DPCD over Aux Chan</strong></td>
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<td><strong>Transmit Training Pattern 1 symbols over Main Link</strong></td>
<td><strong>Checks if CR is achieved</strong></td>
<td></td>
</tr>
</tbody>
</table>

- **Source select Voltage Swing and Pre-Emphasis for TPS1**
- **Hot Plug**
- **Sink Function**
- **Repeat if CR if not done; Otherwise: Channel EQ.**
- **Source Writing Voltage Swing and Pre-Emphasis Levels that will be used for Link Training to Sink DPCD Registers**
Connection Sequence – Link Training Clock Recovery Sequence

**DisplayPort Source**

- Source Function
- Transactions:
  - Hot Plug
  - Send EDID over Aux Chan
  - Read Request for Sink DPCD Capabilities over Aux Chan
  - Returns DPCD Capability Registers over Aux Chan
  - Writes Link Configuration Parameters over Aux Chan
  - Transmit Training Pattern 1 symbols over Main Link
  - Write current drive settings to Rx DPCD over Aux Chan
  - Read Request on DPCD - CR Done over Aux Chan
  - Returns CR Status from DPCD over Aux Chan

**DisplayPort Sink**

- Sink Function
- Transactions:
  - Hot Plug
  - Send EDID over Aux Chan

**Source selects Voltage Swing and Pre-Emphasis for TPS1**

- Transmit Training Pattern 1 symbols over Main Link
- Checks if CR is achieved

- Repeat if CR if not done; Otherwise: Channel EQ.

**Verifying Time Duration between Source Writing Voltage Swing and Pre-Emphasis Levels and Reading for CR Done (4.095 msec)**
Connection Sequence – Link Training Clock Recovery Sequence

**DisplayPort Source**
- **Source Function**
- **Transaction**
  - Send EDID over Aux Chan
  - Read Request for Sink DPCD
  - Capabilities over Aux Chan
  - Returns DPCD Capability Registers over Aux Chan
- **Transaction**
  - Writes Link Configuration Parameters over Aux Chan
  - Transmit Training Pattern 1 symbols over Main Link
  - Write current drive settings to Rx DPCD over Aux Chan
- **Transaction**
  - Check if CR is achieved
  - Transmit Training Pattern 1 symbols over Main Link
  - If CR not done, then adjust Voltage Swing and Pre-Emphasis

**DisplayPort Sink**
- **Sink Function**
- **Transaction**
  - Hot Plug
  - Read Request for Sink DPCD
  - Capabilities over Aux Chan
  - Returns DPCD Capability Registers over Aux Chan
- **Transaction**
  - Transmits Link Configuration Parameters over Aux Chan
  - Transmit Training Pattern 1 symbols over Main Link
  - Checks if CR is achieved
  - Transmit Training Pattern 1 symbols over Main Link
  - Checks if CR is achieved

**Source Selects Voltage Swing and Pre-Emphasis for TPS1**
- **Transaction**
  - Repeat if CR if not done; Otherwise: Channel EQ.

**Verifying Clock Recovery Done on all four Lanes**
Connection Sequence – Link Training Channel EQ, Symbol Lock, Interlane Alignment

**DisplayPort Source**

**Source Function**

- Source selects Voltage Swing and Pre-Emphasis for TPS2/3/4

**Transaction**

- Transmit Training Pattern 2/3/4 symbols over Main Link
- Write current drive settings to Rx DPCD over Aux Chan
- Read Request on DPCD – CE, SL, LA Done over Aux Chan
- Returns CE, SL, LA Status from DPCD over Aux Chan
- Transmit Training Pattern 2/3/4 symbols over Main Link
- Repeat if CE, SL, LA not done; Otherwise: Link Training done.

**Sink Function**

- Checks if CE, SL, LA are achieved
- Write current drive settings to Rx DPCD over Aux Chan
- Read Request on DPCD – CE, SL, LA Done over Aux Chan
- Returns CE, SL, LA Status from DPCD over Aux Chan
- Transmit Training Pattern 2/3/4 symbols over Main Link
- Checks if CE, SL, LA are achieved
- Transmit Training Pattern 2/3/4 symbols over Main Link
- Checks if CE, SL, LA are achieved
- Repeat if CE, SL, LA not done; Otherwise: Link Training done.

**DisplayPort Sink**

**Source Writing Training Pattern Set 4 to Sink DPCD Registers**
## Connection Sequence – Link Training Channel EQ, Symbol Lock, Interlane Alignment

**DisplayPort Source**

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<tr>
<th>Source Function</th>
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<th>Sink Function</th>
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<tbody>
<tr>
<td>Source selects Voltage Swing and Pre-Emphasis for TPS2/3/4</td>
<td>Transmit Training Pattern 2/3/4 symbols over Main Link</td>
<td>Write current drive settings to Rx DPCD over Aux Chan</td>
</tr>
<tr>
<td></td>
<td>Read Request on DPCD – CE, SL, LA Done over Aux Chan</td>
<td>Checks if CE, SL, LA are achieved</td>
</tr>
<tr>
<td></td>
<td>Returns CE, SL, LA Status from DPCD over Aux Chan</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transmit Training Pattern 2/3/4 symbols over Main Link</td>
<td>Checks if CE, SL, LA are achieved</td>
</tr>
<tr>
<td></td>
<td>Repeat if CE, SL, LA not done; Otherwise: Link Training done.</td>
<td></td>
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</tbody>
</table>

**DisplayPort Sink**

- Source sets the drive voltages and pre-emphasis.
- Uses existing values established during Clock Recovery.

---

**TELEDYNE LECROY**

- Everywhere you look.
### Connection Sequence – Link Training Channel EQ, Symbol Lock, Interlane Alignment

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<tr>
<td>Source selects Voltage Swing and Pre-Emphasis for TPS2/3/4</td>
<td>Transmit Training Pattern 2/3/4 symbols over Main Link</td>
<td>Checks if CE, SL, LA are achieved</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Repeat if CE, SL, LA not done; Otherwise: Link Training done.</td>
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<tr>
<td></td>
<td>Write current drive settings to Rx DPCD over Aux Chan</td>
<td>Returns CE, SL, LA Status from DPCD over Aux Chan</td>
</tr>
<tr>
<td></td>
<td>Read Request on DPCD – CE, SL, LA Done over Aux Chan</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transmit Training Pattern 2/3/4 symbols over Main Link</td>
<td></td>
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</table>

#### Remarks:
- Source Reads Status of Channel Equalization, Symbol Lock and Inter-Lane Alignment
- Link Training All Done!
**Connection Sequence – Link Training Irregular Conditions**

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<tr>
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<th>Transaction</th>
<th>Sink Function</th>
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<tbody>
<tr>
<td>Source selects Voltage Swing and Pre-Emphasis for TPS2/3/4</td>
<td>Transmit Training Pattern 2/3/4 symbols over Main Link</td>
<td>(\text{Checks if CE, SL, LA are achieved} )</td>
</tr>
<tr>
<td></td>
<td>Write current drive settings to Rx DPCD over Aux Chan</td>
<td>(\text{Returns CE, SL, LA Status from DPCD over Aux Chan} )</td>
</tr>
<tr>
<td></td>
<td>Read Request on DPCD – CE, SL, LA Done over Aux Chan</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Returns CE, SL, LA Status from DPCD over Aux Chan</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Transmit Training Pattern 2/3/4 symbols over Main Link</td>
<td>(\text{Checks if CE, SL, LA are achieved} )</td>
</tr>
<tr>
<td></td>
<td>Repeat if CE, SL, LA not done; Otherwise: Link Training done.</td>
<td>(\text{Clock Recovery and Channel Equalization completed, but Symbol Lock not completed.} )</td>
</tr>
</tbody>
</table>

If CE, SL, LA not Done, then adjust Voltage Swing and Pre-Emphasis

DisplayPort Source

DisplayPort Sink

Source Function

Transaction

Sink Function

Checks if CE, SL, LA are achieved
Connection Sequence – Link Training Irregular Conditions

DisplayPort Source
Source Function
Source selects Voltage Swing and Pre-Emphasis for TPS2/3/4

Transaction
Transmit Training Pattern 2/3/4 symbols over Main Link

DisplayPort Sink
Sink Function
Checks if CE, SL, LA are achieved

Transaction
Write current drive settings to Rx DPCD over Aux Chan

Read Request on DPCD – CE, SL, LA Done over Aux Chan

Returns CE, SL, LA Status from DPCD over Aux Chan

If CE, SL, LA not Done, then adjust Voltage Swing and Pre-Emphasis

Repeat if CE, SL, LA not done; Otherwise: Link Training done.

Transmit Training Pattern 2/3/4 symbols over Main Link

Checks if CE, SL, LA are achieved

Write current drive settings to Rx DPCD over Aux Chan

Returns CE, SL, LA Status from DPCD over Aux Chan

Checks if CE, SL, LA are achieved

Symbol Lock not completed on Lane 0.
### Connection Sequence – Link Training Clock Recovery Sequence - Failure

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<tr>
<td><strong>Source Function</strong></td>
<td><strong>Sink Function</strong></td>
</tr>
<tr>
<td>Send EDID over Aux Chan</td>
<td>Hot Plug</td>
</tr>
<tr>
<td>Read Request for Sink DPCD Capabilities over Aux Chan</td>
<td>Transaction</td>
</tr>
<tr>
<td>Returns DPCD Capability Registers over Aux Chan</td>
<td>Source selects Voltage Swing and Pre-Emphasis for TPS1</td>
</tr>
<tr>
<td>Writes Link Configuration Parameters over Aux Chan</td>
<td>Transmit Training Pattern 1 symbols over Main Link</td>
</tr>
<tr>
<td>Transmit Training Pattern 1 symbols over Main Link</td>
<td>Write current drive settings to Rx DPCD over Aux Chan</td>
</tr>
<tr>
<td>&gt; 100us</td>
<td>Read Request on DPCD - CR Done over Aux Chan</td>
</tr>
<tr>
<td>Returns CR Status from DPCD over Aux Chan</td>
<td>Checks if CR is achieved</td>
</tr>
<tr>
<td>传输出力电压摆幅和预加重</td>
<td>Checks if CR is achieved</td>
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<td>传输出力电压摆幅和预加重</td>
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Sink requests that the Source adjusts Voltage Swing level and pre-emphasis on all four lanes.
Connection Sequence – Link Training Clock Recovery Sequence - Failure

**DisplayPort Source**

**Source Function**

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<td>Transmit Training Pattern 1 symbols over Main Link</td>
<td>Checks if CR is achieved</td>
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<td>Repeat if CR if not done; Otherwise: Channel EQ.</td>
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**DisplayPort Sink**

**Sink Function**

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<td>Checks if CR is achieved</td>
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- Source resends Training Pattern 1 with requested Voltage Swing level and Pre-Emphasis on all four lanes.
Auxiliary Channel Analyzer (ACA) – Link Maintenance

- If Link Training is successful, then Link Maintenance mode.
- Link Training does not guarantee that the link will behave without errors.
- In Link Maintenance mode, the Link Policy function may force a retrain if there is a failure on the link.
- Link retraining is necessary when there is a loss of Clock Lock, Symbol Lock or Inter-Lane Alignment.
- Failure results in an IRQ interrupt using the Hot Plug Detect lead. The interrupt is a low-going pulse.
- Source re-initiates Link Training.
Auxiliary Channel Analyzer (ACA) – Link Maintenance – IRQ Request

**DisplayPort Source**
- Source Function
- Transaction
- Source selects Voltage Swing and Pre-Emphasis for TPS2/3/4
- Transmit Training Pattern 2/3/4 symbols over Main Link
- Write current drive settings to Rx DPCD over Aux Chan
- Read Request on DPCD – CE, SL, LA Done over Aux Chan
- If CE, SL, LA not Done, then adjust Voltage Swing and Pre-Emphasis
- Transmits Training Pattern 2/3/4 symbols over Main Link
- Checks if CE, SL, LA are achieved
- Repeat if CE, SL, LA not done; Otherwise: Link Training done.
- Link Maintenance Mode
- IRQ HPD Interrupt Request

**DisplayPort Sink**
- Sink Function
- Transaction
- Checks if CE, SL, LA are achieved
- Returns CE, SL, LA Status from DPCD over Aux Chan
- Write current drive settings to Rx DPCD over Aux Chan
- Link Training Mode
- IRQ HPD Interrupt Request

Link Training has been completed. Link failure occurs; Interrupt generated Link Training re-initiated.
DisplayPort Connection Sequence
HDCP 2.2 Authentication

Webinar – June – 2017
### HDCP 2.2 Authentication Transactions

<table>
<thead>
<tr>
<th>HDCP Source</th>
<th>Transaction</th>
<th>HDCP Sink</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Source Function</strong></td>
<td></td>
<td><strong>Sink Function</strong></td>
</tr>
<tr>
<td>Initiate HDCP Authen. – AKE-Init</td>
<td>AKE-Send-Certificate</td>
<td></td>
</tr>
<tr>
<td>Verify Signature on Certificate w/ Kpub-Tx</td>
<td>Generate Km Encrypt Km w/ Kpub-Tx</td>
<td>Decryt Km w/ Kpriv</td>
</tr>
<tr>
<td>Verify integrity of SRM Revocation Check</td>
<td>Compute H-Tx and verify H-Tx w/ H-Rx</td>
<td>Computes H using RxCaps and TxCaps</td>
</tr>
<tr>
<td>Store m, Km and E-kh w/ Sink ID</td>
<td>Set Watchdog Timer</td>
<td></td>
</tr>
<tr>
<td>Initiate Locality Check – LC-Init</td>
<td>Compute L compare with L-Prime</td>
<td>Computes Session Key Computes E-dkey</td>
</tr>
<tr>
<td>Computes Session Key Computes E-dkey</td>
<td>Transmits I-dkey</td>
<td>Computes Session Key Verifies Ks with Edkey</td>
</tr>
</tbody>
</table>

- Shows transactions associated with Source sending Master Key, Sink sending H-prime and Pairing information, Source initiating Locality Check, Sink sending L-prime to verify locality check and Source sending Session Key.
HDCP 2.2 Compliance Test – Test Results Viewer
DisplayPort Main Link Protocol

Webinar – June – 2017
DisplayPort Stream Reconstruction in Sink

DisplayPort Source

- Lane 0: Deserializer, Decoder, De-Scrambler
- Lane 1: Deserializer, Decoder, De-Scrambler
- Lane 2: Deserializer, Decoder, De-Scrambler
- Lane 3: Deserializer, Decoder, De-Scrambler

Serial to Parallel Conversion → 8b/10b Decoding → De-Scrambler

De-Skewer → De-Encryption → Separate Main Stream and Secondary Data

Remove Interlane Skewing → Decrypt HDCP

 Phy Layer/Link Layer Boundary

980 Emulating DisplayPort Sink

Secondary Data

Main Stream Data

Link Symbol Clock to Stream Clock Conversion

Unpacking

De-Steering

Assembling Pixels from Lanes

Reconstructing Pixel Data

Unpacking

De-Steering

980 Emulating DisplayPort Sink

DisplayPort Source

DisplayPort Cable
DisplayPort
Main Link View - 980 Capture Viewer
There are 3 separate panels in the Capture Viewer: 1) Event Plot, 2) Data Decode, 3) Link Symbol panel (all lanes).

The panels are all in sync with one another.

Transaction details are shown in Data Decode Details panel.

Event time is left to right (or top to bottom on the Link Symbol Panel).

You can search for events and specific control characters.

You can filter the list to gain a specific view of any one event type or set of event types.
Main Link Framing Protocol Symbols
8.1Gbps Link Rate
DisplayPort Main Link Protocol – One Video Frame

- Video packets occur during the active video period.
- Metadata: Main Stream Attributes (MSA) and Secondary Data Packets (SDP) occur during the vertical blanking period and are identified with Framing control characters.
- Fill characters are zeros for filling up (stuffing) the unused link symbols.
DisplayPort Main Link Protocol – Measuring the Link Symbol Rate

- Measure the time between link symbol clocks (1.235 ns).
- Use the inverse to determine link symbol rate; multiple by 10 to get the link rate. In this example 8.1Gbps/lane.
DisplayPort Main Link Protocol – Video and Vertical Blanking Structure

- Blue areas are the vertical blanking.
- Greenish areas are the video, stuffing and control characters.
- Empty areas are horizontal blanking.
- Greenish areas are the video, stuffing and control characters.
DisplayPort Main Link Protocol – Framing Control Symbols

- Framing control symbols are used to identify the beginning and end of:
  1) Vertical Blanking,
  2) Fill characters,
  3) Secondary Data packets.
DisplayPort Main Link Protocol – Framing Control Symbols

- Showing end of Video Display Frame, beginning of vertical blanking.
- Also showing the horizontal blanking region.
- Horizontal blanking is stuffed with fill characters.
- Fill characters are zeros as indicated on the Link Symbol panel.
Horizontal blanking is preceded by the four (4) character sequence of Blanking Start (BS), Blanking Fill (BF) followed by the VBID.

The VBID data indicates that this blanking period is not Vertical Blanking.
Horizontal blanking is terminated with a Blanking End (BE) control symbol.
DisplayPort Main Link Protocol – Framing Control Symbols

- Showing end of Video Display Frame, beginning of vertical blanking.
DisplayPort Main Link Protocol – Framing Control Symbols

- Showing end of Video Display Frame, beginning of vertical blanking.
- Fill regions are visible as are some of the protocol elements in the vertical blanking region.
DisplayPort Main Link Protocol – Framing Control Symbols

- Showing end of Video Display Frame, beginning of vertical blanking.
- Last video element is preceded by a set of Fill Characters.
- Then the four (4) character sequence of Blanking Start (BS), Blanking Fill (BF) followed by the VBID.
- VBID details shown in Data Decode Details panel indicating Vertical Blanking = Yes.
- Main Stream Attribute (MSA) data also appears once per frame in the Vertical blanking.
- MSA details shown in Data Decode Details panel.
- MSA data indicates the timing parameters and video attributes such as video type (YCbCr), sampling (4:4:4), color depth (10 bit), etc.
- MSA includes the Mvid and Nvid parameters for stream clock regeneration.
- MSA packets are demarcated by the Secondary Data Start (SS) and Secondary Data End (SE) protocol control packets.
Audio Sample Packets are interspersed in the Vertical Blanking (and the horizontal blanking).

- The control elements in the Vertical Blanking (BS,BF,BF,BS,VBID) follow a cadence.
- From a distance we can see where the sample packets are.
Audio Sample Packets occur in the Vertical Blanking and the horizontal blanking.

Audio sample data shown in Data Decode Details panel.

Audio sample packets include the audio and header information about what the audio format is.

Audio Sample packets are demarcated by the Secondary Data Start (SS) and Secondary Data End (SE) protocol control packets.
DisplayPort Main Link Protocol – Audio Sample Packets (2 channel)

- Density of audio sample packets depends on the number of channels, sampling rate, bits per sample and audio format.
- Two (2) Channel LPCM data at 32kHz with 16 bits per sample (example left) will have fewer audio sample packets than 5.1 Channel LPCM audio at 48kHz sampling rate and 24 bits per sample.
DisplayPort Main Link Protocol – Audio Sample Packets (5.1 channel)

- Density of audio sample packets depends on the number of channels, sampling rate, bits per sample and audio format.
- Two (2) Channel LPCM data at 32kHz with 16 bits per sample (example left) will have fewer audio sample packets than 5.1 Channel LPCM audio at 48kHz sampling rate and 24 bits per sample.
Audio Timestamp packets occur once per video frame in the Vertical Blanking.

Audio Timestamp values shown in the Data Decode Details panel.

Maud and Naud values in the Audio Timestamp packet data are used to reconstruct the audio stream’s sampling frequency.

Audio Timestamp packets are demarcated by the Secondary Data Start (SS) and Secondary Data End (SE) protocol control packets.
DisplayPort Main Link Protocol – Audio CTA Infoframe

- Audio (CTA) Infoframe packets occur once per video frame in the Vertical Blanking.
- Audio Infoframe values shown in the Data Decode Details panel.
- Include values for audio format (e.g. LPCM) audio sampling rate (e.g. 48kHz), number of channels and audio bit depth (e.g. 16 bits).
- Audio Infoframe packets are demarcated by the Secondary Data Start (SS) and Secondary Data End (SE) protocol control packets.
- High Dynamic Range (HDR) infoframe, when required, occurs once per frame in the Vertical Blanking.
- HDR values are show in the Data Decode Details panel.
- HDR parameter values enable a UHD display to put itself in the correct mode to produce the intended High Dynamic Range video and imagery.
- HDR Infoframes are demarcated by the Secondary Data Start (SS) and Secondary Data End (SE) protocol control packets.
Scrambler Reset Packets occur in the Vertical Blanking.

Scrambler Reset packets are substituted for the Blanking Start (BS) elements in the symbol sequence.

Scrambler Reset values are necessary to avoid error propagation.

Scrambler Reset packets are demarcated by the Secondary Data Start (SS) and Secondary Data End (SE) protocol control packets.
Main Link Video
Pixel Mapping (Steering) at
8.1Gbps Link Rate on 4 Lanes
DisplayPort Main Link Protocol – Pixel Mapping

- Pixels data values are spread out mapped “steered” on the lanes that are used.
- The video frame is a test pattern SMPTEbar.
DisplayPort Main Link Protocol – Pixel Mapping (8 bit)

- Looking at the first pixel of a frame on a 4K video resolution with a link rate of 8.1 Gbps using four lanes using a color depth of 8 bits per component.
Notice that for 8 bit color depth with 4K video resolution at 60Hz using 4 lanes at 8.1Gbps link rate, the video in a frame is roughly equal to the stuffing fill characters.
DisplayPort Main Link Protocol – Pixel Mapping (8 bit)

- Looking at the first video transfer unit in a frame.
- Notice that the RGB values are uniform across the lanes with a pixel value of B4 representing the color of the first set of pixels in the frame:

<table>
<thead>
<tr>
<th>Lane0</th>
<th>Lane1</th>
<th>Lane2</th>
<th>Lane3</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0–7:0</td>
<td>R1–7:0</td>
<td>R2–7:0</td>
<td>R3–7:0</td>
</tr>
<tr>
<td>G0–7:0</td>
<td>G1–7:0</td>
<td>G2–7:0</td>
<td>G3–7:0</td>
</tr>
<tr>
<td>B0–7:0</td>
<td>B1–7:0</td>
<td>B2–7:0</td>
<td>B3–7:0</td>
</tr>
</tbody>
</table>

### Lane0
- R0: B4
- G0: B4
- B0: B4

### Lane1
- R1: B4
- G1: B4
- B1: B4

### Lane2
- R2: B4
- G2: B4
- B2: B4

### Lane3
- R3: B4
- G3: B4
- B3: B4
Looking at the first video transfer unit in a frame.

Notice that the RGB values are uniform across the lanes with a pixel value of B4 representing the color of the first set of pixels in the frame:

<table>
<thead>
<tr>
<th>Lane0</th>
<th>Lane1</th>
<th>Lane2</th>
<th>Lane3</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0-7:0</td>
<td>R1-7:0</td>
<td>R2-7:0</td>
<td>R3-7:0</td>
</tr>
<tr>
<td>G0-7:0</td>
<td>G1-7:0</td>
<td>G2-7:0</td>
<td>G3-7:0</td>
</tr>
<tr>
<td>B0-7:0</td>
<td>B1-7:0</td>
<td>B2-7:0</td>
<td>B3-7:0</td>
</tr>
</tbody>
</table>

0x00B4 0x00B4 0x00B4 0x00B4
DisplayPort Main Link Protocol – Pixel Mapping (10 bit)

- Looking at the first pixel of a frame on a 4K video resolution at 60Hz with a link rate of 8.1 Gbps using four lanes with 10 bit color depth.
Notice that for 10 bit color depth per component with 4K video resolution using 4 lanes at 8.1Gbps link rate, there are more video elements in a frame than stuffing fill characters.
DisplayPort Main Link Protocol – Pixel Steering (Mapping) (10 bit–4 Lanes)

- Looking at the first video transfer unit in a frame.
- Notice that the RGB values are no longer uniform across the lanes.
- Here is the pixel mapping structure:

<table>
<thead>
<tr>
<th>Lane 0</th>
<th>Lane 1</th>
<th>Lane 2</th>
<th>Lane 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0–9:2</td>
<td>R1–9:2</td>
<td>R2–9:2</td>
<td>R3–9:2</td>
</tr>
<tr>
<td>R0–1:0</td>
<td>G0–9:4</td>
<td>R1–1:0</td>
<td>G1–9:4</td>
</tr>
<tr>
<td>R4–7:0</td>
<td>R5–7:0</td>
<td>R6–7:0</td>
<td>R7–7:0</td>
</tr>
</tbody>
</table>

[Diagram of pixel mapping structure]
### DisplayPort Main Link Protocol – Pixel Steering (10 bit–4 Lanes)

<table>
<thead>
<tr>
<th>Lane 0</th>
<th>Lane 1</th>
<th>Lane 2</th>
<th>Lane 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0-9:2</td>
<td>R1-9:2</td>
<td>R2-9:2</td>
<td>R3-9:2</td>
</tr>
<tr>
<td>R0-1:0</td>
<td>R1-1:0</td>
<td>R2-1:0</td>
<td>R3-1:0</td>
</tr>
<tr>
<td>R4-9:8</td>
<td>R5-9:8</td>
<td>R6-9:8</td>
<td>R7-9:8</td>
</tr>
<tr>
<td>R4-7:0</td>
<td>R5-7:0</td>
<td>R6-7:0</td>
<td>R7-7:0</td>
</tr>
</tbody>
</table>

#### Pixel Steering Values

<table>
<thead>
<tr>
<th>Lane 0</th>
<th>Lane 1</th>
<th>Lane 2</th>
<th>Lane 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Values</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2D0</td>
<td>2</td>
<td>D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0010</td>
<td>1101</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>B</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0000</td>
<td>10B1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0100</td>
<td>0010</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1101</td>
<td>0000</td>
<td></td>
</tr>
</tbody>
</table>

- **B0**: 9:0 | R4: 9:8
- **B1**: 9:0 | R5: 9:8
- **B2**: 9:0 | R6: 9:8
- **B3**: 9:0 | R7: 9:8

- **G0**: 3:0 | B0: 9:6
- **G1**: 3:0 | B1: 9:6
- **G2**: 3:0 | B2: 9:6
- **G3**: 3:0 | B3: 9:6

- **R0**: 1:0 | G0: 9:4
- **R1**: 1:0 | G1: 9:4
- **R2**: 1:0 | G2: 9:4
- **R3**: 1:0 | G3: 9:4

- **R4**: 7:0 | B0: 9:6
- **R5**: 7:0 | B1: 9:6
- **R6**: 7:0 | B2: 9:6
- **R7**: 7:0 | B3: 9:6

---

**Images:**
- DisplayPort GUI interface showing data transmission and pixel steering values.
- Another GUI interface displaying a frame with pixel values for different lanes.

---

**Teledyne LeCroy:**
- `Everywhere you look.`
980 Auxiliary Channel Analyzer – Multi-Stream Transport Messages

- ACA showing MST messages during setup of Multi-Stream nodes.
- MST Side Band message also shown.
980 Capture Viewer – Viewing VCs of Multi-Stream Transport

- View capture of MST virtual channels.
Teledyne LeCroy – DisplayPort Phy & Protocol Testing

DisplayPort Phy Compliance Testing at 8.1Gbps Link Rate

WaveMaster

DisplayPort Protocol Testing at 8.1Gbps Link Rate

980B Test Platform
Thank you for attending

Questions?

Please take the brief survey that follows.

Please contact me, Neal Kendall at: neal.kendall@teledyne.com
If you have any questions.

- We will be announcing additional webinars on the following topics in the coming months:
  - HDCP 2.2 Testing
  - DisplayPort Multi-Stream Transport (MST)
  - DisplayPort 1.4 Protocols (e.g. DSC/FEC)
  - Dynamic High Dynamic Range