

980/M41h/M41d/M42d 6.35 Release

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Overview

This document provides information on Release 6.35 of the firmware for the 980B/M41h/M41d/M42d and for the Advanced Test Platform (ATP) GUI Manager (PC based External Manager Software).

- This release contains the following components:
 - 32 bit and 64bit Debian package for 980 Version 6.35.
 - 64bit Debian package for M41h/M41d/M42dVersion 6.35.
 - hdcp2 sink playback files deb for compliance test.
 - hdmi sink playback files deb for compliance test.
 - atp-api.zip
 - dsc-sink-test-images.zip
 - hdr-lab images deb.
 - Dolby-audio deb
 - Windows GUI installation msi.

Item	FPGA Versions (Changes compared to previous release are in RED)	
	980/M4xx	
	6.30	6.35
DP 1.2 980 Protocol Analyzer Rev D	4.17.85 Build Number: 1	4.17.85 Build Number: 1
DP 1.2 980 Protocol Analyzer Rev E	4.17.85 Build Number: 1	4.17.85 Build Number: 1
DP 1.2 980 Protocol Analyzer Rev E (410)	4.18.42 Build Number: 1	4.18.42 Build Number: 1
DP 1.2 980 Protocol Analyzer Rev F	Version: 4.18.62 Build Number: 1 (06/07/2018 14:14:18 CST) PCB: 6/G rev=6, DP Product Code=2982	Version: 4.18.62 Build Number: 1 (06/07/2018 14:14:18 CST) PCB: 6/G rev=6, DP Product Code=2982
DP 1.4 980 Protocol Analyzer	Version: 4.25.242 Build Number: 1 (05/13/2021 00:00:21 CST) PCB: 2/C rev=1, DP Product Code=2983	Version: 4.25.245 Build Number: 1 (07/16/2021 11:11:21 CST) PCB: 1/B rev=1, DP Product Code=2983
DP 1.4 USB-C Protocol Analyzer (980/M41d)	Version: 4.26.100 Build Number: 1 (05/13/2021 00:00:21 CST) PCB: 1/B rev=1, DP Product Code=2984	Version: 4.26.103 Build Number: 1 (07/18/2021 21:21:21 CST) PCB: 1/B rev=1, DP Product Code=2984
SDI Scope	4.33.7 Build Number: 32	4.33.7 Build Number: 32
HDMI 2.0 980 Video Generator Rev B	Version: 4.34.1 Build Number: 32 (06/19/2017 15:36:00) PCB: 594b rev. B	Version: 4.34.1 Build Number: 32 (06/19/2017 15:36:00) PCB: 594b rev. B
HDMI 2.0 980 Video Generator Rev C	Version: 6.33.0 Build Number: 46 (04/02/2021 15:36:00) PCB: 594b rev. C	Version: 6.33.0 Build Number: 46 (04/02/2021 15:36:00) PCB: 594b rev. C
HDMI 1.4 980 Protocol Analyzer	Version: 4.22.1 Build Number: 57 (05/22/2017) Gen: 3 PCB: 297b/D	Version: 4.22.1 Build Number: 57 (05/22/2017) Gen: 3 PCB: 297b/D
HDMI 2.0 980 Protocol Analyzer	4.22.7 Build Number: 43	4.22.7 Build Number: 43
HDMI 2.0 RX/TX	Version: 4.27.1 Build Number: 55 (07/12/2018) Gen: 5 PCB: 594d/C	Version: 4.27.1 Build Number: 55 (07/12/2018) Gen: 5 PCB: 594d/C
HDMI 2.1 RX/TX (980/M41h)	Dual GW: 1. Version: 5.30.1 Build Number: 16 (05/04/2021) Gen: 5 PCB: 1200a/C(980); 1200a/E(M41h) 2. Version: 5.30.1 Build Number: 135 (04/25/2021) Gen: 5 PCB: 1200b/C(980); 1200b/E(M41h)	Dual GW: 1. Version: 5.30.1 Build Number: 21 (06/18/2021) Gen: 5 PCB: 1200a/C(980); 1200a/E(M41h) 2. Version: 5.30.1 Build Number: 178 (06/29/2021) Gen: 5 PCB: 1200b/C(980); 1200b/E(M41h)
Phy and Protocol Aux Channel Analyzer	5.16.24 Build Number: 12	5.16.24 Build Number: 12
DP 2.0 USB-C (M42d)	Version: 4.27.132 Build Number: 1 (06/08/2021 17:17:21 CST) PCB: 2/C rev=1, DP Product Code=2985	Version: 4.27.158 Build Number: 1 (07/16/2021 11:11:21 CST) PCB: 2/C rev=1, DP Product Code=2985

1. Installation

Important Note: When upgrading the 980/M41x/M42d system firmware, please be sure to disconnect any video cables that are connected to the 980/M41x Protocol Analyzer / Video Generator modules. Failure to do so may result in issues during upgrade.

Always begin by installing the Windows External Manager software:

1. Download the Windows External Manager 6.35 file R_atpmgr_6.35_Win32.msi.
2. Double-click or Run this file to install it.

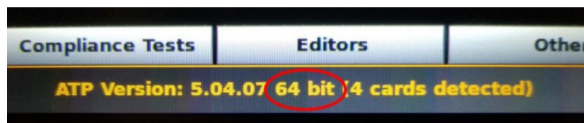
Then install the Instrument Firmware Release.

Important Note:

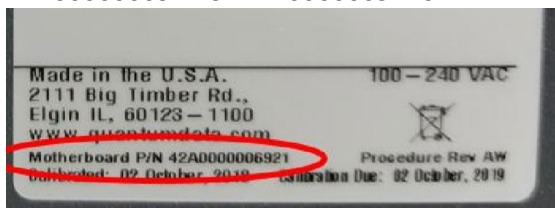
For the M41d/h/M42d series, there is only one Debian file beginning with m4series. This Debian file is for all M41d/h/M42d series devices.

For the 980 series, two different versions of the Instrument Firmware are available, for 32-bit and for 64-bit operating systems. Please make one or both of the following checks to determine whether you need the 64-bit firmware:

3. At the bottom of the instrument Card Control screen, check for “64 bit” indication:



4. On the product label on the back (980B) or bottom (980R) of the instrument, check for Motherboard P/N 42A000006921 or 42A0000009220:



If the ATP version shows 64 bit, or if the label shows either of the above part numbers, then download the “980-atp-64” firmware. Otherwise, you have a 32-bit system, so download the “980-atp-32” firmware.

1. Download the release “980-atp-xx” .deb firmware file as indicated above.
2. Launch the newly installed External Manager (ATP Manager) and connect to the 980 via Ethernet TCP/IP.
 - a. Note: you may see a warning about version mismatch. This is normal and indicates that you should continue with the version upgrade before using the instrument with the new version of the External Manager.
3. From the External ATP Manager program, Navigator section, select **Instruments** -> **Install** -> **Install UI/Firmware/Gateway**. Browse to and select the 980-atp-xx or m4series release file for your product, select Open, and continue with the process. The test instrument will power down at the end.
IMPORTANT: On some products it can take up to 15 minutes to program the FPGA, so watch the progress and do not remove power before the process is complete.

If the 980/ M41d/h/M42d is licensed for **HDR Lab** Images (License 45):

4. Download the HDR Lab Images .deb file.
5. From the External ATP Manager program, Navigator section, select **Instruments** -> **Install** -> **Upgrade System Components**. Browse to and select the hdr-lab-images.deb file, select Open and continue with the process.

If the 980/ M41d/h/M42d is licensed for **HDMI HDCP CTS 2.3 Compliance Test for Sinks** (License 29):

6. Download the atp-hdcp2-sink-ct.deb file.
7. From the External ATP Manager program, Navigator section, select **Instruments** -> **Install** -> **Install CT Scripts**. Browse to and select the atp-hdcp2-sink-ct.deb file, select Open and continue with the process.

If the 980/ M41h is licensed for **HDMI CTS 1.4b Compliance Test for Sinks** (License 6) or HDMI CTS 2.0 Package 4 Sink Tests (License 27):

8. Download the atp-hdmi-sink-ct.deb file.
9. From the External ATP Manager program, Navigator section, select **Instruments** -> **Install** -> **Install CT Scripts**. Browse to and select the atp-hdcp2-sink-ct.deb file, select Open and continue with the process.

If the 980/ M41h is licensed for **HDMI DSC Compliance Test of Sink, 980/M41h (License 79)**

10. Download dsc-sink-test-images.deb file.
11. From the External ATP Manager program, Navigator section, select **Instruments** -> **Install** -> **Upgrade System Components**. Browse to and select the **dsc-sink-test-images.deb** file, select Open and continue with the process.

To update the system Dolby audio files, perform the following steps.

12. Download the dolby-audio.deb .deb and av-sync.deb files.
13. From the External ATP Manager program, Navigator section, select **Instruments** -> **Install** -> **Upgrade System Components**. Browse to and select the dolby-audio.deb file, select Open and continue with the process.
14. Then repeat the previous step with the av-sync.deb file.

2. Release Notes

2.1. Resolved Issues and New features

Ticket No.	Description - DisplayPort
V980-4492	M42d DSC configuration and defaults.
V980-4629	API returns ValueError for tlqd.TlqdGetFormatParameters(qdDev, all=True)
V980-4579	Release 6.30 980 Embedded GUI DPCD Editor doesn't show right-hand side properly
V980-4628	GUI: Real-time Adaptive Sync Timing Analyzer support
V980-4578	HFR2-16, HF2-37, and HF2-38 show up as not approved in GUI in release 6.30
V980-4606	Need generator GUI change to switch between new UHBR link training and old method of link training
V980-4607	Need Analyzer GUI change to switch between Legacy and UHBR capability on M42D
V980-4635	CDF Imports into Navigator go into DP Adaptive-Sync Sink folder
V980-4637	Need GUI change to support Adaptive Sync Timing CDF change.
V980-4599	Implement SCR to 4.7.3.2 EDID Read with Greater than 8 Blocks of Data.
V980-4612	M42d software down load fails during regular upgrade procedure.
V980-4561	Source DUT Adaptive-Sync test
V980-4627	TMDS Sink CT Y420 Video CDF issue
V980-4636	64-bit MB unit HDMI/DP generators output wrong BMP color values
V980-4533	DPCD registers 0005 and 2205 can't be set with different values

Ticket No.	Description - HDMI
V980-4643	HF1-25 doesn't test timings declared in Source non 2160p Video Formats Above 340 Timings
V980-4024	HF2-94 does not run properly with Rev B HDMI 2.0 Generator
V980-4590	SCDC timing issue for HFR1-11, 1-19, 1-20, 1-21
V980-4641	eARC test HFR5-2-26 and -27 fail for valid time of COMMA sequences after HPD=0
V980-4595	CVTEM packets captured for non-DSC test vectors
V980-4568	PS5 fails HF1-58 due to MVRR and timing measurement
V980-4570	HF1-58 Failing in FRL mode for 4Kx60
V980-4576	Report Register 0x3748 Return
V980-4618	HFR1-10 failure seems incorrect
V980-4621	Support a mode where FLT_no_retrain bit is never set when enabling DSC generator
V980-4626	Output multiple VSIFs simultaneously
V980-4622	8K DSC source tests get stuck at "preprocess 1 frames" and don't finish
V980-4592	HDMI FRL HFR1_18 failures in API
V980-4593	API HDMI TMDS HF1_33 automation failures
V980-4594	QD980 SW GUI Manager hangs during HDMI2.1 48G/FRL tests execution
V980-4620	API needs a method for retrieving and parsing the incoming eARC signal type
V980-4632	HDMI FRL Source HFR1-22 question

2.2. Unresolved Issues

Ticket No.	Description - DisplayPort
V980-4084	The M42d may exhibit Image flickering and HBR3 Symbol errors with a DP1.4 input stream.
V980-4083	The M42d may exhibit problems authenticating with DP 1.4 sources in both HDCP 2.3 and 1.3.
V980-4063	The M42d may show an HDCP compliance failure HDCP2.3 for the 1A-01 & 1B-01 tests with an error: AUTH:Timer Expired to receive ENC_EN.
V980-4049	On the M42d, part of the secondary data packets (SDP) can get lost and not shown in the capture.
V980-3844	The M42d pixel error test report may not show all errors that occur.
V980-4448	DP1.4/2.0: TX & RX CRC values are not equal when units connected back-to-back
V980-3794	The M41d Video Generator function may not detect MST topology correctly.
V980-4013	The M42D sometimes will incorrectly set the output to four (4) MST Streams when the Sink indicates supports for only a single MST stream.
V980-3993	The 980 DP 1.4 modules and the M41d indicate decoding errors in 1 or 2 lane mode errors from a source when HDCP 1.3 is in use.
V980-4452	M42d Corrupted Realtime video but Good Capture
V980-4372	Restrict programming of M4xx PMU to when release's version number is higher than programmed version
V980-4655	M42d Generator: With 10k format, Bottom of image is bad/missing.
V980-4664	M42D analyzer Vstream process crashed when switch from 8k DSC image to 2K Dsc image. This affects DSC source CTS and DSC validation for any source DUT.
Ticket No.	Description - HDMI
V980-3939	On the 980 48G module, some of the TMDS source compliance tests require that the user re-initiate the selection of the video format.
V980-3839	On the 980 48G module Tx, the VRR signal may become unstable after about 10 minutes.
V980-3308	The 980 48G HDMI 2.1 module and the M41h the eARC RX: Selecting "SPDIF Output" "ON" on M41h gives extraneous errors.
V980-4028	On the 980 and M4 series products, the Aux Channel Analyzer (ACA) utility may improperly indicate time gaps between the Rx and Tx ports. timing shows several hours gap between RX & TX ports.
V980-4389	HDMI 2.1 analyzer pixel error test shows lots of errors
V980-4393	Snow or black video is output from HDMI 2.1 generator when changing FRL link rate with HDCP 2.3 enabled
V980-3937	HF1-66 inconsistent test results
V980-4146	AVI IF tests like HF1-51 fail incorrectly due to an issue with AVI IF check
V980-4605	HFR1-80 through 83 Pass although a failure message is indicated during execution

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2.3. New Display Port Features/Enhancements in 6.35

New Display Port Related features

M42d now supports the following:

- Adaptive sync timing info
- Adaptive sync src LL CT
- 20G support without passive probing.
- LTTTPR source detection and 8b/10b LT
 - non LTTTPR
 - Transparent LTTTPR
 - non transparent LTTTPR
- LTTTPR source detection and 128b/132b non transparent LT

2.3.1. Adaptive Sync Timing information now available

You may now view the timing variations with Adaptive Sync in the snapshot view.

To begin the process, click the timing button on the left hand side of the window. Changes in Vtotal will be reflected on the dashboard under Total: and will appear in the timing window itself as Min, Max and Avg. Changes in Vtotal Min, Max and Avg for the session will be displayed as well.

If the user wishes a history of changes, these are accumulated in an ASCII log file in the following location:

/home/qd/timing_history.log” on the M42d

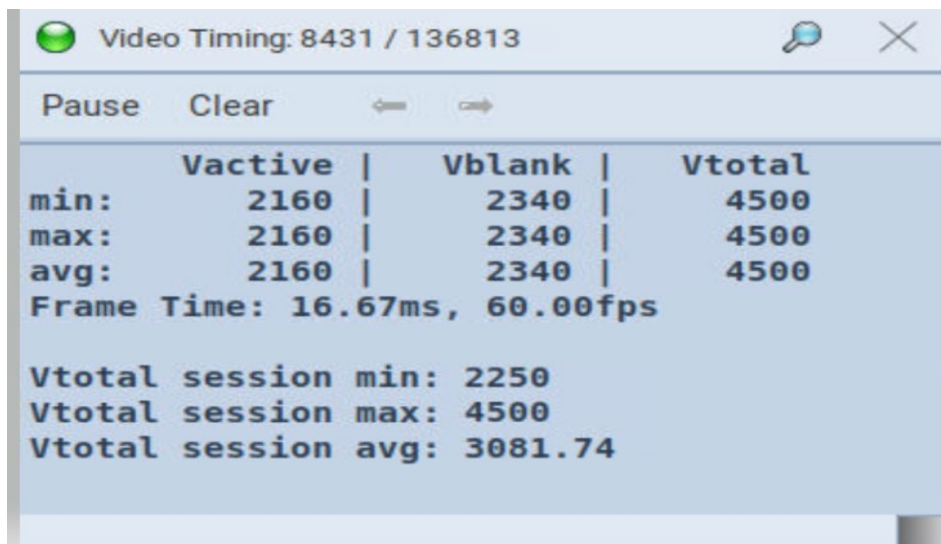
The current default measurement period is 1 second, and it can be changed by using the Linux command”

echo <accumulation period in seconds> /proc/driver/AS_TIMING_DP20

Example:

```
echo 2 > /proc/driver/AS_TIMING_DP20
```

This command will change the measurement period to 2 seconds

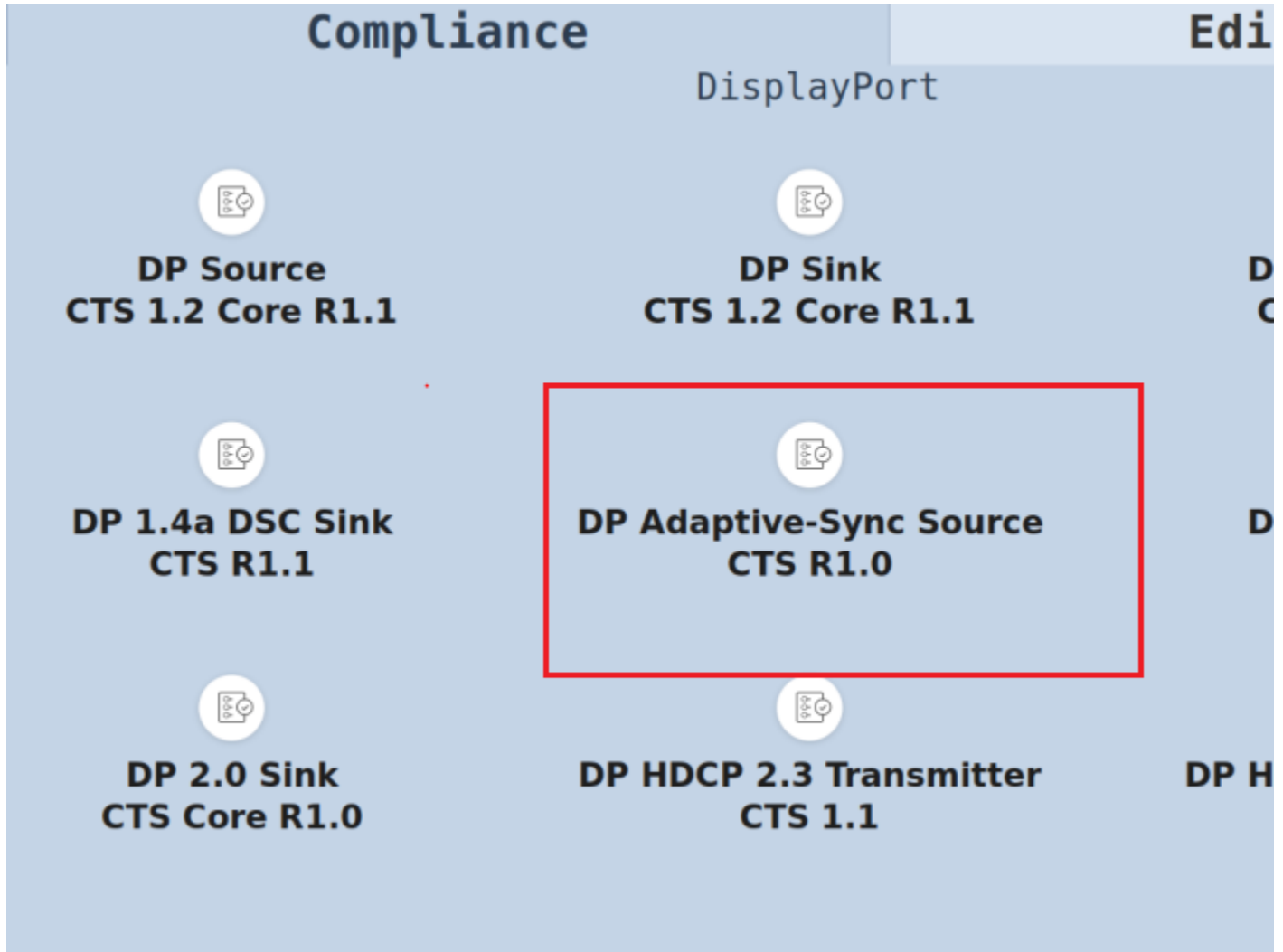


2.3.2. Adaptive Sync Source LL CT

These compliance tests are a licensed feature. The current tests available are:

- 4.8.1.1 Fixed Average VTotal Support over Declared Frame Rate Range
- 4.8.1.2 Duration Increase Constraint Value Support.

The tests can be accessed from the Compliance Tab of the M42d. Control of the test actions are settable in the CDF.



2.3.3. 20G Link Rate Support

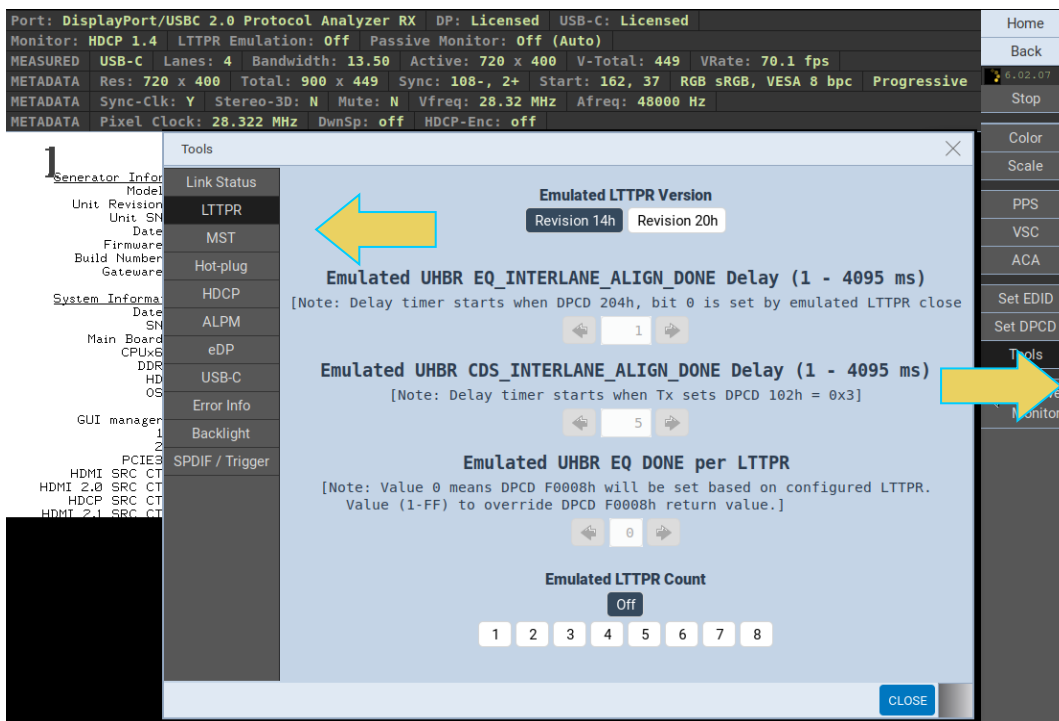
The M42d now supports the 20G link rate for all standard operations. *Please note: For this release, the Passive Probing option is not functional at 20G link rate. It will be added in a future release.*

2.3.4. LTTPR Enhancements

All LTTPR testing features are licensed. The M42d supports the testing of LTTPR-capable source devices and also provides link layer transaction data for LTTPR devices and a DPRx sink. Two revisions of LTTPR are supported, revisions 14h and 20h. Revision 14h is for non-transparent mode or transparent mode for LTTPR in an 8b/10b network. Revision 20h is used when testing LTTPRs in non-transparent mode in UHBR networks.

While testing a source device in the non-transparent mode, each LTTPR is trained in the link. This ensures better signal quality to the end-to-end link. When testing an LTTPR-capable source device, the M42d can emulate a network of up to 8 LTTPR devices and a DPRx (sink). The M42d can also generate video to LTTPR device(s) as a DPTx (source).

The tool you will use for LTTPR emulation is located within the **Protocol Analyzer Rx** interface, accessible from the Home screen of the M42d's embedded ATP Manager GUI. To access the LTTPR utility, click the **Tools** icon in the control menu on the right-hand side of the Receiver. This will display the **Tools** dialog box. Click the **LTTPR** tab on the left sidebar to access the utility, as demonstrated below.



The LTTPR emulation tool appears as shown above. Using this tool, you can emulate up to eight LTTPR devices. This tool offers options for configuring the emulated LTTPR, and more configurations are available within the DPCD Editor.

For full details on use of the LTTPR Feature please see the M42d Users guide Version A2, Section 8: LTTPR Testing located at:

https://www.quantumdata.com/assets/m42d_ug.pdf

2.4. New HDMI Features/Enhancements in 6.35

New Display Port Related features

980 HDMI 2.1 and M41h now supports the following:

- Bug fixes

3. Support

For further information on the quantumdata 980/M41h/M41d/M42d products and the ATP Manager please see the Quick Start and Users guides available on our website at: <https://www.quantumdata.com>

For support on the quantumdata 980 or other Teledyne LeCroy PSG products, please send an email to: psgsupport@teledynelecroy.com

Please include your full contact information and a detailed description of the problem, including product model number, serial number, firmware version, software version, and any trace files pertaining to the issue.

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