Essentials of HDMI 2.1 Protocols for 48Gbps Transmission

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Agenda

◆ Brief review of HDMI 1.4/2.0 protocols.
◆ New features of HDMI 2.1.
◆ Fixed Rate Link (FRL) Packetization.
  ◆ FRL Structure
  ◆ Packetization of TMDS data.
◆ Reed Solomon Forward Error Correction (FEC).
◆ Link Training for Fixed Rate Link transmission.

◆ Future webinar topics for HDMI 2.1:
  ◆ Enhanced Audio Return Channel (eARC)
  ◆ Display Stream Compression (DSC)
Background
HDMI 1.4/2.0 TMDS Protocol
HDMI 2.0 Anatomy - Review

- Three (3) TMDS channels carry the video data, metadata, control data, etc.
- HDMI 1.4/2.0 has a separate clock channel.
- DDC channel bus carries HDCP transactions, EDID exchange and SCDC reads/writes.
Audio, metadata, data islands are placed in the horizontal and vertical blanking periods.

Control periods (in gray) are preamble data; control periods occur between audio and metadata in the video blanking.

Guard bands occur before and after data islands and before video data.
HDMI 2.0 Protocol Capture

- Capture Viewer has two panels:
  - Graphical Event Plot
  - Data Decode Table.
- Timestamps are shown on both panels.
- Time goes left to right on Event Plot and top to bottom the Data Decode window.
- Zoomed out view with all the frames in a capture visible.
- Vsync pulses and encryption enable pulses are visible per frame.
- TMDS and Hsync are not distinguishable.
HDMI 2.0 Protocol Capture
HDMI 2.0 Protocol Capture
Control periods (preamble) occur between audio and metadata in the blanking.

Guard bands occur before and after data islands and before video data.
HDMI 2.0 Protocol Capture

- Zoomed in to show Data Islands and their preambles and guard bands.
HDMI 2.1 Features
HDMI 2.1 – Data Transmission

- Supports higher bit rates (higher resolutions), up to 12Gbps/lane (48Gbps over 4 lanes in FRL mode). This doubles the signaling rate over each transmission pair (6G to 12G).

- Higher data rates achieved by:
  - A new cable category (Cat 3 “48G”) being defined and a new connector specification.
  - New line coding 16b/18b to allow greater bandwidth while still maintaining DC balance.
  - Adds a new data channel (“lane”) in “FRL” mode by repurposing the TMDS clock channel. HDMI 2.1 uses and embedded clock derived from the transmitted data.

- Uses packet-based protocol (Fixed Rate Link [FRL]):
  - FRL permits the data to be transmitted over the link at only a few data rates to simplify the Receiver clock recovery function. (HDMI 1.4 & 2.0 allowed a near continuum of TMDS rates.)
  - FRL requires Forward Error Correction (FEC).
  - FRL requires a link training mechanism which uses the Status and Control Data Channel (SCDC) registers. FRL Link Training is controlled by the sink; sets the link rate & number of lanes.

- Display Stream Compression (DSC) is a visually lossless compression technique that offers a range of compression up to 3:1 compression.

- Enhanced Audio Return Channel (eARC) to support a richer set of audio formats including Dolby TrueHD and Atmos, greater channel counts and sampling rates for LPCM. Discovery and configuration of eARC is simplified; no more reliance on CEC bus.
HDMI 2.0 vs HDMI 2.1 Channel/Lane Usage

- Uses packet-based protocol -- Fixed Rate Link (FRL).
- Adds a new data channel (“lane”) by repurposing the TMDS clock channel. HDMI 2.1 uses an embedded clock when in FRL mode derived from the transmitted data.
HDMI 2.1 FRL Stream Construction in Source (4 Lane Example)

HDMI Source ▸ Optional ▸ Display Stream Compression ▸ HDCP Encryption ▸ FRL Packetizer ▸ Forward Error Correction (FEC) Encoding & Mapping ▸ FEC Parity Mapper ▸ FEC Encoder ▸ Scrambler ▸ 16b/18b Encoder ▸ Serializer ▸ HDMI Link

FRL Packet Structure

Super Block

Character Block

Character Block

Character Block

Character Block

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

FRL Pkt

TMDS Data
HDMI 2.1 – Fixed Rate Link (FRL) Facts

- FRL Super Blocks contains four (4) Character Blocks.
- FRL Character Blocks contain one or more FRL packets.
- FRL Character Blocks are comprised of up to 510 FRL characters.
- Eight (8) of the 510 FRL characters carry FEC parity.
- FRL packets can span more than one (1) Character Block.
- FRL packets cannot span more than one Super Block.
- FRL packets encapsulate the three (3) TMDS channels.
- There are three (3) FRL packet (“Map”) types:
  - Gap – single FRL fill character.
  - Active Video – Video and Guard band.
  - Video Blanking; three (3) categories of data:
    - Control periods (preamble) for video and data islands
    - Data island data
    - Data island guard bands (leading and trailing).
HDMI 2.1 Protocol Analyzer

- Zoomed way out on this view.
HDMI 2.1 Protocol Analyzer

- Zoomed in view.
- TMDS data elements are shown on the top of the upper graphical panel.
- FRL packet elements are shown in the bottom portion of the upper graphical panel.
- Details of the selected item in the table view are shown in the lower panel.
- Four (4) Lane data shown in the lower Data Details Panel.
HDMI 2.1 Protocols
FRL Super Blocks

Note: All example captures use FRL 4 lane mode with a 1080p60 TMDS stream
There are four (4) Character Blocks in each Super Block.

Character Blocks are composed of FRL Packets.

Start Super Blocks (SSB) are used by a receiver for character alignment.

SSB characters are not scrambled. They are special 18b codes.

SSB characters are distributed across all four (4) FRL lanes.

SSB characters are always preceded RS FEC parity data.
FRL Packetization – Super Blocks, Scrambler Reset

- FRL transmission requires scrambling.
- Synchronous scramblers send resets periodically to aid the receiver in recovering the data.
- In FRL transmission the scrambler is reset with Scrambler Reset (SR) characters in Super Blocks.
- Sources transmit the Start Super Block Characters (SSB) for 32 Super Blocks, followed by the SR Character for one Super Block (Red).
- SR characters are across all four (4) lanes.
- The SR characters are not themselves scrambled.
Character Blocks are comprised of 510 FRL characters.

Each Character Block has eight (8) FEC characters.

For the Video Blanking each FRL character transports at least one (1) video blanking period TMDS tri-bytes.

For the Active Video, three (3) 16 bit FRL characters transport two (2) TMDS active video tri-bytes (24 bits).
Character Blocks can contain any of the 3 types of FRL packets:
- Active Video.
- Video Blanking.
- Gap.

Active Video FRL packets contain the TMDS video and video guard bands.

Video Blanking FRL packets contain data islands, including infoframes, audio samples, guard bands and preambles, control characters, V/Hsync.

Gap characters are used to fill unused bandwidth e.g. 1080p TMDS video (~4.5Gbps) into a 48Gbps FRL stream.
HDMI 2.1 Protocols
Active Video FRL Packets
The first Active Video FRL packet of each video line contains video guard band data.
FRL Packetization – Active Video Packets; Video Guard Band

- Zoomed in view showing Active Video Guard Band.
FRL Packetization – Active Video Packets; FRL Packet Header

- Showing Active Video Guard Band and the Active Video FRL Packet header.

```
S0000 10 01 0110 1001
```

Hex = 02    Hex = 169

Type = 02 = Active Video

Length = Hex 169 = 361d
FRL Packetization – Active Video Packets with Video Guard Band

- Zoomed in view showing Active Video Guard Band.
FRL Packetization – Active Video Packet Distribution

- Zoomed out to see how the Active Video packets are distributed in a line of video.
- Example shows a 1080p TMDS video stream (~4.5Gbps) encapsulated into a 48Gbps FRL stream.
- There are a lot of fill characters (“Gap characters”) required to occupy unused bandwidth.
- **Note**: Only a sample of the video pixel data is shown in the Detail Data panel.
HDMI 2.1 Protocols
Video Blanking FRL Packets
We are going to zoom in to take a look at how the Video Blanking FRL Packets are populated.
Video Blanking FRL packets can contain video preamble (control periods), Data Island Guard Band (leading and trailing) and Data Island data.

**Video Blanking Characters:** 137

1 – FRL Blanking Header
32 - Video Preamble (Control)
8 – Data Island Preamble
2 – Data Island Guard Band
32 – Data Island Data
2 – Data Island Guard Band
60 - Video Preamble
---
137 FRL Characters
FRL Packetization – Video Blanking FRL Packets; FRL Packet Header

- Example shows Gap and Video Blanking FRL packets with Video Preamble (Control Period) characters.
- Video Blanking FRL packet header indicates the Type and the Length.
- Starts on 1063 byte of the Super Block.

Video Blanking FRL Packet Header

```
0000 11 00 1000 1001
Hex = 03    Hex = 089
Map Type = 03 = Video Blanking
Length = Hex 089 = 137d
```
FRL Packetization – Video Blanking FRL Packets; Preamble (Control Period)

- Example shows Gap, Video Blanking and Video Preamble FRL characters (Control Period).

Example shows Gap, Video Blanking and Video Preamble FRL characters (Control Period).

Video Preamble (Control Period) Characters:
0 0 0 2 0
0000 0000 0010 0000
FRL Packetization – Video Blanking FRL Packets; Data Island Preamble

- Example shows Data Island Preamble Characters (TMDS CTL0/2 Characters).

```
0000 0100 0010 0000
```

- Data Island Preamble Characters:
  - CTL0: 0
  - CTL2: 4
  - Lane 0: 2
  - Lane 1: 4
  - Lane 2: 0
  - Lane 3: 0

0 4 2 0
0000 0100 0010 0000
FRL Packetization – Video Blanking FRL Packets; Data Island Data Guard Band

- Example shows Data Island guard band.
FRL Packetization – Video Blanking FRL Packets; Data Island Data

- Example shows Data Island data (AVI InfoFrame data).
FRL Packetization – Video Blanking FRL Packets; Video Preamble

- Example shows Video Preamble (Control Period) Characters.
All Video Blanking FRL packets have to be transmitted in a blanking period before any Active Video is transmitted.

Note: You can have all three (3) types of FRL packets within a single Character Block (example not shown).
HDMI 2.1 Protocols
Video Blanking FRL Packets
Horizontal and Vertical Sync
FRL Packetization – Video Blanking FRL Packets; **Full Hsync Pulse**

- Hsync Control occurs in Video Blanking FRL packets.
- Example shows entire Hsync (44 FRL Characters) within single Vertical Video Blanking FRL packet.

![Diagram showing FRL Packetization](image)

```plaintext
0000 0000 0010 0001
```

Hsync & Video Preamble

0 0 2 1
0000 0000 0010 0001

Lane 0  Lane 1  Lane 2  Lane 3

CTL0  Hsync
FRL Packetization – Video Blanking FRL Packets; **Split HSync**

- Horizontal Video Sync ("pulse") can be **split** between Blanking FRL packets, Character Blocks and Super Blocks.
- Video Preambles are also **split** between FRL packets, Character Blocks and Super Blocks.

Hsync pulse split between two FRL packets: 24 and 20 Characters
- Zoomed in view.
- Vertical Sync shown.
- Blanking end shown.
- Active video starts.
FRL Packetization – Video Blanking FRL Packets; Vertical Sync

- Zoomed out view.
- Video Vertical Sync (“pulses”) are split between several Video Blanking FRL packets, Character Blocks and Super Blocks.
FRL Packetization – Video Blanking FRL Packets; Vertical Sync

- Zoomed in view.
- Vertical Video Sync ("pulse") are split between Video Blanking FRL packets, Character Blocks and Super Blocks.
- Each consumes the entirety of an FRL blanking packet (136 of the 137 ([the 1 left over is the FRL header byte])).
HDMI 2.1 Protocols
Forward Error Correction
Reed Solomon Forward Error Correction (FEC) – How Does it Work?

- Two (2) polynomials are used to generate RS code words.
  1) Primitive Polynomial – The Finite Field (Galois Field) generating polynomial. An irreducible (polynomial equivalent of an integer prime number - cannot be factored).
  2) RS Code Generator Polynomial – The polynomial used to encode the code words in the four (4) FEC encoders.

(1) Finite Field “Primitive” Polynomial

Lower Order polynomials of Field Generating Polynomial

(2) Encoding Polynomial (FEC Parity Encoder 0)
(2) Encoding Polynomial (FEC Parity Encoder 1)
(2) Encoding Polynomial (FEC Parity Encoder 2)
(2) Encoding Polynomial (FEC Parity Encoder 3)

FRL Character Block Data

HDMI

Decoding Polynomial
No Remainder
Decoding Polynomial
No Remainder
Decoding Polynomial
No Remainder
Remainder (Yes)

Lookup Table (Uses remainder value to identify & correct error)
- FEC blocks are appended to each Character Block.
- There are eight (8) 16 bit blocks of FEC data.
- Reed Solomon corrects up to 2 symbols errors per block.
- Sinks have a counter in the SCDC registers with the FEC errors that Sources can read.
- FEC-ER records show FEC errors that have been corrected.
- The following are indicated:
  - Super block byte number e.g. 1072.
  - Lane number of the error, e.g. Lane 0.
  - RS encoder number, e.g. 0 or 1.
  - Whether the RS symbol was one of the “natural” or “swapped.”
- Note: “Swapped” and “Natural” designations only occur in 4 Lane mode.
FRL Packetization – FRL Elements with FEC Error Correction

- Example showing “Swapped” errors.
- The following are indicated:
  - Super block byte number e.g. 2904.
  - Lane number of the error, e.g. Lane 0.
  - RS encoder number, e.g. 2 & 3.
  - Whether the RS symbol was one of the “natural” or “swapped.”
- Note: “Swapped” and “Natural” designations only occur in 4 Lane mode.
HDMI 2.1 Fixed Rate Link (FRL) Link Training

Webinar – December – 2017
FRL Link Training – Aux Channel Protocol Transaction Capture

- Two panels:
  - Event Transaction Panel.
  - Details panel.
- Details of the highlighted item in Event (Transaction) Panel is shown in the Details Panel
- Timestamps applied to all events.
FRL Link Training Rules and Link Training Sequence

- Link training is required for Fixed Rate Link (FRL) transmission.
- Link training is required when first initializing a link or when changing the link rate.
- Link training establishes the link rate, equalization and character lock.
- Link training uses the Status and Control Data Channel (SCDC) register reads and writes over the DDC.
- Link training must be completed within 200 ms for one link rate.
- Link training uses specific bit pattern sequences selected by the sink.
- Sources must support all link training patterns; sinks can request any pattern.
- Link Training progresses through: LTS:1 → LTS:2 → LTS:3 → LTS:P (possibly LTS:4)

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<th>SCDC (DDC) Transaction</th>
<th>Sink Function</th>
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<td>Source verifies Max_FRL_Rate in HDMI Forum Vendor Specific Data Block of the sink EDID</td>
<td>LTS:1</td>
<td>Source Reads EDID over DDC Sink Returns EDID to Source</td>
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<td>Source queries Status Flags for Link Training Ready</td>
<td>LTS:2 – Source prepares for link training</td>
<td>Source polls Sink for FLT_Ready</td>
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<td>Source writes to Config Registers to set FRL rate and number of lanes for Link Training</td>
<td>LTS:3 – Source initiates Link Training</td>
<td>Source sets FRL_Rate and No. of Lanes</td>
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<td>Source polls Update Flags for FLT Update to start Link Training</td>
<td>LTS:4 – Sink requests new Link Rate</td>
<td>Source polls every 2ms for FLT_Update</td>
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<tr>
<td>Source continues polling Status Flags for Link Training Pattern &amp; Status and Link Training Pattern Request</td>
<td>LTS:P - Link Training is completed</td>
<td>Source polls Sink for Link Training Pattern Request</td>
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<tr>
<td>Source transmits at requested rate</td>
<td></td>
<td>Sink requests no link training pattern – go to LTS:P</td>
</tr>
<tr>
<td>Source transmits FRL data</td>
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<td>Sink sets FLT_Update flag</td>
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<td>Sink requests Link Training at new rate</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sink sets FRL_Start to receive FRL data</td>
</tr>
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</table>
FRL Link Training LTS:1 – Source Reads Sink EDID to Verify FRL Support

Source Function

- Source verifies Max_FRL_Rate in HDMI Forum Vendor Specific Data Block of the sink EDID
- Source queries Status Flags for Link Training Ready
- Source writes to Config Registers to set FRL rate and number of lanes for Link Training
- Source polls Update Flags for FLT_Update to start Link Training
- Source continues polling Status Flags for Link Training Pattern & Status and Link Training Pattern Request
- Source transmits at requested rate
- Source transmits FRL data

SCDC (DDC) Transaction

- Source Reads EDID over DDC
- Sink Returns EDID to Source
- Source polls Sink every 2ms for FLT_Update
- Source writes to Config Registers to set FRL rate and number of lanes for Link Training
- Source polls Update Flags for FLT_Update to start Link Training
- Source transmits at requested rate
- Source transmits FRL data

HDMI Sink

Sink Function

- Sink sets Status Flags to indicate ready for Link Training
- Sink requests Link Training Test Pattern (Test Pattern Lanes are independent)
- Sink requests no link training pattern - go to LTS:P
- Sink sets FLT_Update flag
- Sink requests Link Training Test Pattern Request
- Sink requests No Link Training Test Pattern to indicate Pass
- Sink sets FRL_Start to receive FRL data
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LTS:1 – Source prepares for link training

- Source prepares for link training

LTS:2 – Source initiates Link Training

- Source initiates Link Training

LTS:3 – Source requests new Link Rate

- Source requests new Link Rate

LTS:4 – Link Training is completed

- Link Training is completed

Source starts 200ms Timer

Sink requests Link Training Test Pattern Request

Sink requests Link Training Test Pattern Request

Sink requests Link Training Test Pattern Request
FRL Link Training – Source Reads Sink EDID to Verify FRL Support

- LTS:1
- EDID is read to verify that the HDMI sink supports FRL.
- Max_FRL_Rate must be set.
FRL Link Training – Source Reads Sink EDID to Verify FRL Support

- LTS:1
- HDMI Forum Vendor Specific Data Block must indicate Max FRL Rate, Example 12Gbps on 4 Lanes.
- SCDC_Present must also be set.
### FRL Link Training LTS:2 – Source Polls Sink for FLT Ready (Ready to Link Train)

#### SCDC (DDC) Transaction

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<td>Source transmits at requested rate</td>
<td>Sink requests Link Training at new rate</td>
</tr>
<tr>
<td>Source transmits FRL data</td>
<td>Sink sets FRL_Start to receive FRL data</td>
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**LTS:1**
- Source Reads EDID over DDC
- Sink Returns EDID to Source

**LTS:2 – Source prepares for link training**
- Sink sets Status Flags to indicate ready for Link Training

**LTS:3 – Source initiates Link Training**
- Source polls Sink every 2ms for FLT_Update
- Source polls Sink for Link Training Pattern Request
- Sink requests no link training pattern – go to LTS:P

**LTS:4 – Sink requests new Link Rate**
- Source sets new FRL_Rate (if Sink Requests)

**LTS:P - Link Training is completed**
- Sink requests Link Training at new rate
- Sink sets FRL_Start to receive FRL data
FRL Link Training – Source Polls Sink for FLT Ready (Ready to Link Train)

- **LTS:2**
- Source queries Sink for FLT Ready flag set in SCDC Status register.
- FLT Ready = Set indicates that Sink is ready for Link Training.)
FRL Link Training LTS:2 – Source Sets FRL Lane Rate and Number of Lanes

HDMI Source Function:
- Source verifies Max_FRL_Rate in HDMI Forum Vendor Specific Data Block of the sink EDID
- Source queries Status Flags for Link Training Ready
- Source writes to Config Registers to set FRL rate and No. of lanes for Link Training
- Source polls Update Flags for FLT_Update to start Link Training
- Source continues polling Status Flags for Link Training Pattern & Status and Link Training Pattern Request

SCDC (DDC) Transaction:
- LTS:1
  - Source Reads EDID over DDC
  - Sink Returns EDID to Source
- LTS:2 – Source prepares for link training
  - Source polls Sink for FLT_Ready
  - Source sets FRL_Rate and No. of Lanes
- LTS:3 – Source initiates Link Training
  - Source polls Sink every 2ms for FLT_Update
  - Sink requests Link Training Pattern Request
  - Sink requests no link training pattern – go to LTS:P
- LTS:4 – Sink requests new Link Rate
  - Source sets new FRL_Rate (if Sink Requests)
- LTS:P – Link Training is completed
  - Source polls Sink for FRL_Start and FLT_Update
  - Source transmits FRL data

HDMI Sink Function:
- Sink sets Status Flags to indicate ready for Link Training
- Source polls Sink for Link Training Pattern Request
- Sink sets FLT_Update flag
- Source sets new FRL_Rate (if Sink Requests)
- Sink requests Link Training Pattern (Test Pattern Lanes are independent)
- Sink requests No Link Training Test Pattern to indicate Pass
- Sink requests Link Training at new rate
- Sink sets FRL_Start to receive FRL data

[Diagram showing the flow of interactions between HDMI Source and Sink with specific steps and timelines marked.]
FRL Link Training – Source Sets FRL Lane Rate and Number of Lanes

- LTS:2
- Source sets link rate and number of lanes for link training by writing to SCDC Configuration registers.
FRL Link Training LTS:3 – Source Starts Timer; Reads Sink Registers for LT Pattern

- **Source Function**
  - Source verifies Max_FRL_Rate in HDMI Forum Vendor Specific Data Block of the sink EDID
  - Source queries Status Flags for Link Training Ready
  - Source writes to Config Registers to set FRL rate and number of lanes for Link Training
  - Source polls Update Flags for FLT Update to start Link Training
  - Source continues polling Status Flags for Link Training Pattern & Status and Link Training Pattern Request
  - Source transmits at requested rate
  - Source transmits FRL data

- **SCDC (DDC) Transaction**
  - LTS:1
    - Source Reads EDID over DDC
    - Sink Returns EDID to Source
  - LTS:2 – Source prepares for link training
    - Source polls Sink for FLT_Ready
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    - Source sets new FRL_Rate (if Sink Requests)
  - LTS:P - Link Training is completed
    - Source polls Sink for FRL_Start and FLT_Update
    - Sink requests Link Training at new rate
  - Sink sets FRL_Start to receive FRL data

- **Sink Function**
  - Sink sets Status Flags to indicate ready for Link Training
  - Sink starts 200ms Timer
  - Sink requests Link Training Test Pattern (Test Pattern Lanes are independent)
  - Sink requests No Link Training Test Pattern to indicate Pass
  - Sink sets FRL_Start to receive FRL data
FRL Link Training – Source Starts Timer; Reads Sink Registers for LT Pattern

- **LTS:3**
- Sink requests link training test pattern for each lane by setting SCDC Status flag registers in response to Source read.
- Example shows Lane 0 uses LPT4 and Lane 1 uses LPT5.
FRL Link Training – Source Starts Timer; Reads Sink Registers for LT Pattern

- **LTS:3**
- Sink requests link training test pattern for each lane by setting SCDC Status flag registers in response to Source read.
- Example shows Lane 2 uses LPT6 and Lane 3 uses LPT7.
### FDL Link Training LTS:4 – Source Starts Timer; Reads Sink Registers for New Lane Rate

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<td>Sink requests No Link Training Test Pattern to indicate Pass</td>
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<td>Sink requests Link Training at new rate</td>
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<td>Sink sets FRL_Start to receive FRL data</td>
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</table>

**200ms**
TLT:4
- Sink requests change in the link rate.
FRL Link Training LTS:4 – Source Tries New Lane Rate

<table>
<thead>
<tr>
<th>HDMI Source</th>
<th>SCDC (DDC) Transaction</th>
<th>HDMI Sink</th>
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<td><strong>Source Function</strong></td>
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<tr>
<td>Source verifies Max_FRL_Rate in HDMI Forum Vendor Specific Data Block of the sink EDID</td>
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<td>Source Reads EDID over DDC Sink Returns EDID to Source</td>
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<tr>
<td>Source queries Status Flags for Link Training Ready</td>
<td></td>
<td>Sink sets Status Flags to indicate ready for Link Training</td>
</tr>
<tr>
<td>Source writes to Config Registers to set FRL rate and number of lanes for Link Training</td>
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<td>Source starts 200ms Timer</td>
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<tr>
<td>Source polls Update Flags for FLT Update to start Link Training</td>
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<td>Source continues polling Status Flags for Link Training Pattern &amp; Status and Link Training Pattern Request</td>
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<td><strong>LTS:4 – Sink requests new Link Rate</strong></td>
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<td>Source sets new FRL_Rate (if Sink Requests)</td>
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<tr>
<td><strong>LTS:P - Link Training is completed</strong></td>
<td></td>
<td>Source sets new FRL_Rate (if Sink Requests)</td>
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<td>Source polls Sink for FRL_Start and FLT_Update</td>
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FRL Link Training – Source Tries New Lane Rate

- LTS:4
- Source sets link rate to 10Gbps on 4 lanes and re-initiates FRL link training by writing to SCDC Config register.
FRL Link Training LTS:3 – Link Training Successful, Sink Does Not Request LT Pattern

**HDMI Source Function**
- Source prepares for link training
- Source initiates Link Training
- Source verifies Max_FRL_Rate in HDMI Forum Vendor Specific Data Block of the sink EDID
- Source queries Status Flags for Link Training Ready
- Source writes to Config Registers to set FRL rate and number of lanes for Link Training
- Source polls Update Flags for FLT_Update to start Link Training
- Source continues polling Status Flags for Link Training Pattern & Status and Link Training Pattern Request
- Source transmits at requested rate
- Source transmits FRL data

**SCDC (DDC) Transaction**
- Source reads EDID over DDC
- Sink returns EDID to Source
- Source polls Sink for FLT_Ready
- Source sets FRL_Rate and No. of Lanes
- Source polls Sink every 2ms for FLT_Update
- Source writes to Config Registers to set FRL rate and number of lanes for Link Training
- Source polls Sink for FRL_Start and FLT_Update

**HDMI Sink Function**
- Sink sets Status Flags to indicate ready for Link Training
- Sink sets FLT_Update flag
- Sink requests Link Training Test Pattern (Test Pattern Lanes are independent)
- Sink requests no link train pattern → LTS:P
- Sink requests No Link Training Test Pattern to indicate Pass
- Sink sets FRL_Start to receive FRL data
- Sink requests Link Training at new rate

**Timeline**
- Source starts 200ms Timer
- Sink requests Link Training Test Pattern (Test Pattern Lanes are independent)
- Sink requests No Link Training Test Pattern to indicate Pass
- Sink sets FRL_Start to receive FRL data
FRL Link Training – Link Training Successful, Sink Does Not Request LT Pattern

- **LTS:3**
- Link training is successful when Sink indicates no link training test pattern in the SCDC status flags.
- Example shows Lanes 0 and 1.
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FRL Link Training – Link Training Completed, Sink Sets FRL_Start

- LTS:P
- Sink indicates link training completed and is ready to receive FRL data (FRL_Start flag is set).
- LTS:P
- Source queries SCDC Update registers every 2 msecs to determine if FLT_Update is set indicating need to re-Link Train.
Source queries SCDC Update registers every 2 msecs.
Example shows read from source.
Link Maintenance – SCDC Query

- Source queries SCDC Update registers every 2 msecs.
- Example shows reply from sink.
Thank you for attending

Please contact me, Neal Kendall at: neal.kendall@teledyne.com
If you have any questions.

- We will be announcing additional webinars on the following topics in the coming months; possible topics are:
  - HDMI 2.1 Display Stream Compression (DSC)
  - HDMI 2.1 Enhanced Audio Return Channel (eARC)
  - DisplayPort 1.4 Protocols (e.g. DSC/FEC)
  - Dynamic High Dynamic Range