

quantumdata[™] 980

DisplayPort 1.4 / USB-C / eDP Video Generator / Protocol Analyzer Video Generation and Analysis Testing up to 8.1Gb/s Link Rates Link, FEC & DSC Compliance Suites now Approved!



Key Features

- Run DisplayPort functional tests and protocol compliance tests up to full DP 1.4 specification
- Equipped with both DP standard and USB-C ports for Tx and Rx function—all test features supported through either type of connector
- View Power Delivery (PD) negotiations for USB-C DP Alt Mode
- Run functional tests on displays and monitors up to 8.1 Gb/s link rates with large format and test pattern library
- Generate Display Stream Compression (DSC) select patterns and configure slices and video parameters
- Configure link training parameters to test display's handling
- View EDID and DPCD registers
- Access DSC Test CRC registers for automated verification of source DSC compression
- Test DP sources up to 8.1 Gb/s link rates; view incoming video and meta-data—including DSC compressed--from a source device in real time
- Capture and decode incoming video, protocol and control packets—including Display Stream Compression (DSC)
- UPDATE! Run DP 1.4 EDID compliance tests on sink devices
- Monitor Aux Channel transactions as a DP source or sink
- Passively monitor Aux Channel between a source & display even at 8.1Gb/s link rates
- Run DP 1.4 Link Layer compliance tests on sources and sinks up to 8.1 Gb/s link rates
- NEW! Run DP 1.4 EDID compliance tests on sinks
- Run DP 1.4 Forward Error Correction (FEC) compliance tests
- Run DP 1.4 Display Stream Compression compliance tests for sources and sinks
- Run DCP-approved HDCP 2.2 compliance tests on DisplayPort sources, sinks and repeaters
- Run audio tests using programmable LPCM sine wave audio tones and compressed formats
- Run tests on embedded DisplayPort (eDP) 1.4b sources and panels using fast link training and ALPM
- Test eDP backlight control functions on panel using either backlight control pins or Aux Channel control commands

The Teledyne LeCroy quantumdata 980 DP1.4/USB-C/eDP Video Generator/ Analyzer module provides an unprecedented combination of functional and compliance testing for video, audio and protocol of DisplayPort devices. The module supports 1.62, 2.7, 5.4 & 8.1 Gb/s data rates on 1, 2 & 4 lanes on its Tx video generator port and its Rx analyzer port for both the standard DP ports and the new USB-C ports with DP Alt Mode.

The module's protocol analyzer supports real time analysis and deep analysis using captures of incoming DisplayPort streams from source devices including DSC/FEC compressed streams. The module's video generator can be used for testing displays, USB-C adapters, extenders, etc. The module is equipped with all the standard video timings and test patterns necessary for testing modern displays.

The 980 DP 1.4 Video Generator / Protocol Analyzer module supports a full suite of link layer and NEW! EDID compliance tests for both sources and sinks including compliance tests for forward error correction (FEC).

The full-size DP and USB-C Tx and Rx ports support Auxiliary Channel analysis of the DP Aux Channel, and the USB-C ports support Aux Channel Analysis of the USB-C Configuration Channel. An included Aux Chan monitoring board supports passive monitoring of the DP aux channel via full-size DisplayPort connectors, between a source and display. This enables analysis of link training and HDCP interoperability between devices.

For developers of Embedded DisplayPort (eDP), the new module offers the hardware necessary to support a variety of optional eDP features. Initial support includes fast link training, alternate scrambler seed, Advanced Link Power Management (ALPM) and Tx backlight control. A pin header is available to provide access to the backlight Tx control test feature.

The module can be equipped in the 980B Test Platform and controlled either through the embedded 980 GUI Manager or the PC-based GUI Manager

Source Testing

The 980 DP 1.4 Video Generator / Analyzer module emulates a DP display device (sink) for analyzing source devices. There are two options for the analysis function for testing DisplayPort source devices:

- Basic Analyzer Provides real time viewing of video and metadata for functional testing.
- Capture/Store Protocol Analyzer Provides capture and store of the main link including protocol and control packets, main stream attributes and secondary data.

Display Testing

The 980 DP 1.4 Video Generator / Analyzer module supports video, audio and protocol functional testing of highend DP displays. The module supports 1.62, 2.7, 5.4 & 8.1 Gb/s data rates on 1, 2 & 4 lanes on both its Tx ports and its Rx ports.

The module also supports DP 1.4 Link Layer HDCP 2.2 compliance testing for DisplayPort source, sink and repeater devices and link layer compliance testing for sink devices.

DISPLAY TESTS – VIDEO/AUDIO TESTING

Video Generation

The 980 DP 1.4 Video Generator / Analyzer module supports video and audio functional testing at link rates up to 8.1 Gb/s on 1, 2 and 4 lanes to support high resolution formats. The module has an extensive set of video formats and library of test patterns. You can set any pattern in motion to test motion artifacts with the Image Shift feature.



Test Setup for Sink Test

Link Training Control and Configuration

The module's link training control feature enables you to configure the link training parameters during testing. You can set limits on the lane count and link rate and allow the link training engine to establish link training based on those limitations or you can force link training parameters—lane count, link rate, voltage swing, pre-emphasis.

Link Training Control and Configuration



Alt Mode Negotiation

The USB Type C Transmit connector participates in discovery, power contract negotiation, and DP Alt Mode negotiation. The protocol messages can be monitored on the Auxiliary Channel Analyzer (right).

Format Selection

	Fo	mat							DD/US	DC
CTA	VESA	Fold	ler	Lists	EDID				Gene	ra
уре		Reso	ution		Frame Rate	Aspect	CVT2560H			Ī
TVC	640		768	800	24	Ratio				
VR	848	900	960	1024	30	4:3				
MT	1064	1152	1224	1280	43					
MR	1360	1366	1400	1440	48	5:4				
	1536	1600	1680	1704	50	11:5				
	1728		1800	1856	60	16:9				
	1864	1920	2048	2128		16:10				
	2304	2456	2560	2728	75					
		3840			85					

Audio Testing

The module offers a programmable LPCM audio sine wave generator enabling you to set the number of channels (up to 8), the amplitude, frequency, sampling rate and bit depth for uncompressed formats.

LPCM Audio Testing





Aux Channel Analyzer – DP Alt Mode Negotiation

DISPLAY TESTS - PROTOCOL TEST FEATURES

Protocol Testing

The 980 DP 1.4 Video Generator / Analyzer module offers a variety of features for testing DisplayPort protocols. You can verify HDCP 1.3 and HDCP 2.2 authentication transactions between the module's Tx port and a DP display. The module's EDID Decode feature enables you to examine the EDID of the connected display. The DPCD Decode feature enables you to examine the DPCD registers of the connected display. You can read the EDID and/or the DPCD of downstream MST nodes.



Test Setup for Sink Test

Multi-Stream Transport

The DP 1.4 Video Generator / Analyzer module emulates an MST source for testing an MST branch device or MST-capable monitor. Up to four (4) streams are supported with a depth of one. The Auxiliary Channel Analyzer (ACA) utility depicts the MST negotiations with the connected MST Rx device.

Auxiliary Channel Analyzer

The 980 DP 1.4 Video Generator / Analyzer module's Auxiliary Channel Analyzer (ACA) feature enables you to monitor the DP Aux Channel for link training and MST negotiations, HDCP transactions and EDID exchanges between the DP 1.4 module and a connected display. The ACA logs these events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

Aux Channel Analyzer – Link Training

Op	en Clo	se Export	Options	Filter	Find			P
31	My_DP_AC	A_Capture] Eve	nts: 356 (1331))				
0	DPHP	DP-110	+00:30:45	915707	HPD Falling Edge	 Start Time: +00:30:50.871183 		2
1	DPHP	DP-210	+00:30:50	867851	HPD Rising Edge	7ype: Native		
2	DPHP	DP-210	+00:30:50	.867851	HPD Falling Edge	Direction: Reply		
3	DPHP	DP-T10	+00:30:50	867852	HPD Rising Edge	Reply by Read Remore		
4	DNAT	DF-710	+00:30:50	868068	> R:200 SINK_COUNT L=6	Repry to Read Request.		
5	DNAT	DF-710	+00:30:50	.868141	< ACK 41 04 00 00 80 00	02200: DP1 3 DPCD REV		
6	DNAT	DF-710	+00:30:50	.870824	> R:E TRAINING AUX RD_INTERVAL L=1	Bit Name Va.	ue Description	
7	DNAT	DP-110	+00:30:50	.870897	< ACK 81	***** *********************************		
8	DNAT	DP-210	+00:30:50	.870966	> R:0 DFCD_REV L=1	3-0 Minor Revision		
9	DNAT	DP-710	+00:30:50	871039	< ACK 14	7-4 Major Revision	•	
10	DNAT	DP-710	+00:30:50	871110	> R:2200 DP1.3_DPCD_REV L=16	02201: MAX LINE BATE		
11	DNAT	DF-T10	+00:30:50	.871183	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08	Bit Name Va.	ue Description	
12	DNAT	DF-210	+00:30:50	871393	> R:90 FEC_CAPABILITY L=1	***** *********************************		
13	DNAT	DF-710	+00:30:50	.871466	< ACK BF	7-0 MAX_LINK_RATE 11	ih 8.1 Gbps/lan	18
14	DNAT	DP-710	+00:30:50	871544	> R:60 DSC SUPPORT L=15	00000, Mar 1998		
15	DNAT	DP-710	+00:30:50	.871617	< ACK 01 21 03 7F FB 07 01 00 00 1F 0E EE	Bit Name Va	ue Description	
16	DNAT	DF-710	+00:30:50	871906	> R:D eDP_CONFIGURATION_CAP L=1			
17	DNAT	DP-710	+00:30:50	.871979	< ACK 00	4-0 MAX_LANE_COUNT	4 lanes	
18	DNAT	DP-110	+00:30:50	872047	> R:701 EDP_GENERAL_CAPABILITY_1 L=1	5 POST_LT_ADJ_REQ_SUP N(1)	
19	DNAT	DP-110	+00:30:50	.872120	< ACK 87	6 TPS3_SUPPORTED Y(2	
20	DNAT	DP-T10	+00:30:50	872188	> R:702 EDP_BACKLIGHT_ADJ_CAPS L=1	/ ENHANCED_FRAME_CAP I(1	
21	DNAT	DF-110	+00:30:50	.872261	< ACK 22	02203: MAX DOWNSPREAD		
22	DNAT	DF-710	+00:30:50	872331	> R:725 EDP_PWMGEN_BIT_COUNT_MIN L=2	Bit Name Val	ue Description	
23	DNAT	DF-710	+00:30:50	.872403	< ACK 02 0C			
24	DNAT	DF-710	+00:30:50	872482	> R:2E RX_ALPM_CAPABILITIES L=1	0 MAX_DOWNSPREAD	Up to 0.5%	
25	DNAT	DP-210	+00:30:50	872554	< ACK 03	1 STREAM_REGEN_STATUS_CAP N(Reserved	
26	DNAT	DF-710	+00:30:50	.872624	> W:116 RX_ALPM_CONFIGURATION L=1 01	3	Reserved	
27	DNAT	DP-710	+00:30:50	.872704	< ACK	4	Reserved	
28	DHDCP	DP-710	+00:30:50	873436	> R:69493 R#Status L=1	5	Reserved	
29	DHDCP	DP-710	+00:30:50	873509	< ACK 00	6 NO AUX HANDSHAKE LINK TRAINING N (2	
30	DPLT	DF-110	+00:30:50	935325	> R:100 LINK_BN_SET L=2	/ TPS4_SOPPORTED I(1	
31	DPLT	DF-710	+00:30:50	935398	< ACK 1E 04	02204: NORP		
32	DNAT	DF-710	+00:30:51	.030734	> R:200 SINK_COUNT L=6	Bit Name Val	ue Description	~
33	DNAT	DF-710	+00:30:51	.030807	< ACK 41 04 00 00 00 00	< C		>

EDID Decode View

Generator												-		\times
Mode: SST 👻	DP:	Lic FN	ar:2160	p60 080m				P-R	ate:594.00M	Hz F-Rat	e:60.00Hz	Output	Discor	nnect
(97) 3840x21	160p @ 1	60 Hz	16:9										Refr	esh
					Pat						Tools		DP/USE	RC 1 4
Link Train	Read	Save	Load	Edit									Gener	rator
ALPM	Block	#00												
Backlight	Block	Type:	Base E	DID										
	Vers	ion 1	header	verifi	ed									
DPCD Viewer		Manut	facture	r: QDI	(0204b)									
HDCP Test		11004	Serial	#: 17 (00000011	h)								
EDID Decode	EDID V	Moo /ersion	iel Yea n l, Ré	r: 2017 vision	4									
EDID Comp	Number	of ac	iditior	al bloc	ks: 1									
Image Shift														
Image Ctrl														
DSC														
Editors														
Corinte														
	Block	ج 1	/2 >	Page	< 1/1	0 >								
													CLOS	E

DPCD Register View

Generator							-	
Mode: SST + (97) 3840x21	DP:Lic FM USBC:Lic IM 50p @ 50 Hz 1	n:2160p6 G:SmpteB 16:9) ar 3840x2	160 Pi	E-Rate:594.00MHz rogressive RGB-Sbpc	F-Rate:60.00Hz H-Rate:135.00kHz	Output	Disconnect Refresh
	Format		Pattern		Audio	Tools		DP/USBC 1.4
Link Train ALPM Backlight	Receiver Capability 00000-0008F		READ AL	Receiv	AD PAGE REPORT er Capability 00-0008F		0	Generator
USB-C DPCD Viewer	Link Config. 00100-001C2	00000: D Bit	PCD_REV Name	Value	Description			
HDCP Test	Link/Sink Status 00200-002FF	7-4 3-0 00001: M Bit	MAJOR REV MINOR REV AX_LINK_RATE Name	1 4 Value	Description			
EDID Comp Image Shift Image Ctrl	Test Automation 00218-00282	7-0 00002: M	MAX_LINK_RATE	14h	5.4 Gbps/lane			
DSC Editors Scripts	Source Specific 00300-003FF Sink	Bit 4-0 5 6 7	Name MAX LANE COUNT POST_LT_ADJ_REQ_SUP TPS3_SUPPORTED FUNDAVEND FRAME_CAR	Value 4 N(0) Y(1) V(1)	A lanes			
	Specific 00400-004FF Branch	00003: M Bit	AX_DOWNSPREAD Name	Value	Description			
	Specific 00500-005FF	0 1 2	MAX_DOWNSPREAD STREAM_REGEN_STATUS_CAP	1 N(0) 0	Up to 0.5% Reserved			
	Sink Control 00600	3 4 5 6	NO BIT HANDSHAFF LINK TRAINING	0 0 0	Reserved Reserved Reserved			
	eDP Backlight 00700-0074F	7 00004: N Bit	TP54_SUPPORTED	Y(1) Value	Description			
	AV						~	CLOSE

HDCP 2.2 Test

SOURCE TESTS – CAPTURE & DECODE FOR DEEP

Capture and Decode

The 980 DP 1.4 USB-C Video Generator / Analyzer captures and decodes the main link attributes in order to diagnose interoperability issues related to them. The Protocol Analyzer captures & stores main link data and provides visibility into main stream attributes, secondary data elements, K-Characters and protocol errors. The Protocol Analyzer presents these elements on a graphical timeline and in a table. You can search for data and select any transaction in the table to view its details. The capture utility also enables you to capture specific MST streams from the source.

DP Alt Mode Negotiation

The 980 DP 1.4 USB-C Generator / Analyzer USB-C Rx connector participates in discovery, power contract negotiation, and DP Alt Mode negotiation. The protocol messages can be monitored on the Auxiliary Channel Analyzer.





Capture and Decode (Filter View showing only Audio Packets)



DP Connection Sequence with DP Alt Mode Negotiations

Ope	en Close	Export	Options	Filter	Find		,e
[A	A_980-USE	to-LMon-USB	_w-PSV-CBL]	Events: 416			
0	DPHP	DPUSBC-T61	+69:49:57	.040950	HPD Falling Edge Start Time: +69:49:58.431054		
1	PDVDM	DPUSBC-T61	+69:49:58	.375607	'PRT:0 Discover Identity 5 Start of Packet: SOP		
2	PDCTL	DPUSBC-T61	+69:49:58	.376363	'CBL:0 GoodCRC Message Type: Vendor_Defined		
3	PDVDM	DPUSBC-T61	+69:49:58	.378497	'CBL:0 ACK Discover Identity MessageID: 2		
4	PDCTL	DPUSBC-T61	+69:49:58	.379712	'PRT:0 GoodCRC Port Power Role: Sink		
5	PDDTA	DPUSBC-T61	+69:49:58	.380969	SRC:0 Source_Capabilities Spec_Revision: Revision 2.0		
6	PDCTL	DPUSBC-T61	+69:49:58	.381662	SNK:0 GoodCRC Data Objects: 4		
7	PDDTA	DPUSBC-T61	+69:49:58	.382411	SNK:0 Request 1) VDM Header		
8	PDCTL	DPUSBC-T61	+69:49:58	.383112	SRC:0 GoodCRC SVID or VID : 0xFF00 (65280)		
9	PDCTL	DPUSBC-T61	+69:49:58	. 384599	SRC:1 Accept VDM Type : Structured		
10	PDCTL	DPUSBC-T61	+69:49:58	.385162	SNK:1 GoodCRC VDM Version : 1.0		
11	PDCTL	DPUSBC-T61	+69:49:58	.414898	SRC:2 PS_RDY Command Type : ACK		
12	PDCTL	DPUSBC-T61	+69:49:58	.415460	SNK:2 GoodCRC Command : Discover Identity		
13	PDCTL	DPUSBC-T61	+69:49:58	.416481	SNK:1 PR_Swap 2) ID Header VDO		
14	PDCTL	DPUSBC-T61	+69:49:58	.417031	SRC:1 GoodCRC Data Capable as USB Host : Yes		
15	PDCTL	DPUSBC-T61	+69:49:58	.418538	SRC:3 Reject Data Capable as a USB Device: Yes		
16	PDCTL	DPUSBC-T61	+69:49:58	.419094	SNK:3 GoodCRC Product Type : Undef	ined	
17	PDVDM	DPUSBC-T61	+69:49:58	.429721	SRC:4 Discover Identity USB Vendor ID : 0x043	3E	
18	PDCTL	DPUSBC-T61	+69:49:58	.430407	SNK:4 GoodCRC 3) Cert Stat VDO		
19	PDVDM	DPUSBC-T61	+69:49:58	.431054	SNK:2 ACK Discover Identity TID: 0x00000		
20	PDCTL	DPUSBC-T61	+69:49:58	.432141	SRC:2 GoodCRC 4) Product VDO		
21	PDVDM	DPUSBC-T61	+69:49:58	.433641	SRC:5 Discover SVIDs USB Product ID: 0x9A30		
22	PDCTL	DPUSBC-T61	+69:49:58	. 434334	SNK:5 GoodCRC bcdDevice : 0x0010		
23	PDVDM	DPUSBC-T61	+69:49:58	.435001	SNK:3 ACK Discover SVIDs		
24	PDCTL	DPUSBC-T61	+69:49:58	.435815	SRC:3 GoodCRC - Preamble: CC-1, 63, [Sync-1,	ic-1,Syn	c-2]
25	PDVDM	DPUSBC-T61	+69:49:58	.437319	SRC:6 Discover Modes - Object 1: FF008041h		
26	PDCTL	DPUSBC-T61	+69:49:58	.438012	SNK:6 GoodCRC - Object 2: C400043Eh		
27	PDVDM	DPUSBC-T61	+69:49:58	.438662	SNK:4 ACK Discover Modes - Object 3: 00000000h		
28	PDCTL	DPUSBC-T61	+69:49:58	.439490	SRC:4 GoodCRC - Object 4: 9A300010h		
29	PDVDM	DPUSBC-T61	+69:49:58	.440990	SRC:7 Enter Mode 1 - CRC: C1B79DE2h		
30	PDCTL	DPUSBC-T61	+69:49:58	.441669	SNK:7 GoodCRC		
31	PDVDM	DPUSBC-T61	+69:49:58	.442360	SNK:5 ACK Enter Mode 1		
20	BD CET	DBUCDO-M61	+60.40.50	442055	STOLE CondCDC		

(Passive) Auxiliary Channel Analyzer

The 980 DP 1.4 Video Generator / Analyzer module's Adjunct Auxiliary Channel Analyzer board enables you to monitor the DP Aux Channel for link training and MST negotiations, HDCP transactions and EDID exchanges between a DisplayPort source and display device. This enables developers to investigate interoperability problems between DisplayPort devices involving link training, HDCP and EDID. Solution is provided using a custom cable provided by Teledyne LeCroy. The ACA logs these events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

UDPATE! SOURCE ANALYSIS & AUX CHANNEL ANALYSIS

Analyzer

The 980 DP 1.4 module's Analyzer enables you to view the incoming video, link rate, timing, colorimetry and various other metadata at a glance. The Analyzer provides a basic confidence test to verify that the incoming video is essentially correct. The Rx port emulates any EDID to test a source devices handling of various EDIDs. You can also configure DPCD registers for emulating on the DP Rx port using the DPCD Editor (below).



Source Test Setup

DPCD Editor

Link Training Status

Real Time Analysis



Aux Channel Analyzer (ACA)

The 980 DP 1.4 module's Auxiliary Channel Analyzer (ACA) feature enables you to monitor the DP Aux Channel for link training, MST negotiations, HDCP transactions and EDID exchanges between the M41d Rx port and a source device. The ACA logs the events and assigns precise timestamps to them. You can view the details of each transaction. These ACA logs can be saved and disseminated for further analysis by colleagues and other subject matter experts.

Auxiliary Channel Analyzer Showing Link Training

Ope	en Clos	se Export	Options	Filter	Find					
- []	AV_DP_AC	A_Capturel Eve	nts: 356 (1331	2						
)	DPHP	DP-T10	+00:30:45	915707	HPD Falling Edge	st	art Time: +00:30:50.871183			
1	DPHP	DP-710	+00:30:50.	867851	HPD Rising Edge		Type: Native			
2	DPHP	DP-710	+00:30:50	867851	HPD Falling Edge	D	Direction: Reply			
3	DPHP	DP-710	+00:30:50.	867852	HPD Rising Edge	March 100 Au	Command: ACK			
6	DNAT	DP-710	+00:30:50	868068	> R:200 SINK COUNT L=6	webry co	neau nequest.			
5	DNAT	DP-710	+00:30:50	868141	< ACK 41 04 00 00 80 00	02200 1	P1 3 DPCD REV			
5	DNAT	DP-710	+00:30:50	870824	> R:E TRAINING AUX RD_INTERVAL L=1	Bit	Name	Value	Description	
7	DNAT	DP-710	+00:30:50	870897	< ACK 81					**
4	DNAT	DP-710	+00:30:50	870966	> R:0 DFCD_REV L=1	3-0	Minor Revision	4		
	DNAT	DP-710	+00:30:50	871039	< ACK 14	7-4	Major Revision	1		
,0	DNAT	DP-210	+00:30:50	871110	> R:2200 DP1.3 DPCD_REV L=16	02201: N	GAX LINK RATE			
1	DNAT	DP-T10	+00:30:50	871183	< ACK 14 1E C4 81 01 00 01 80 00 20 04 08	Bit	Name	Value	Description	
2	DNAT	DP-710	+00:30:50	871393	> R:90 FEC_CAPABILITY L=1					-
3	DNAT	DP-T10	+00:30:50.	871466	< ACK BF	7-0	MAX_LINK_RATE	1Eh	8.1 Gbps/lan	ŧ
4	DNAT	DP-710	+00:30:50.	871544	> R:60 DSC SUPPORT L=15					
5	DNAT	DP-T10	+00:30:50	.871617	< ACK 01 21 03 7F FB 07 01 00 00 1F 0E EE	Rit	Name	Value	Description	
6	DNAT	DP-710	+00:30:50	871906	> R:D eDP_CONFIGURATION_CAP L=1					k
7	DNAT	DP-710	+00:30:50	871979	< ACK 00	4-0	MAX_LANE_COUNT	4	4 lanes	
8	DNAT	DP-T10	+00:30:50.	872047	> R:701 EDP_GENERAL_CAPABILITY_1 L=1	5	POST_LT_ADJ_REQ_SUP	N(0)		
9	DNAT	DP-T10	+00:30:50	.872120	< ACK 87	5	TPS3_SUPPORTED	Y(1)		
D	DNAT	DP-T10	+00:30:50	872188	> R:702 EDP_BACKLIGHT_ADJ_CAPS L=1		ENRANCED_FRAME_CAF	1(1)		
1	DNAT	DP-710	+00:30:50	.872261	< ACK 22	02203: N	DOWNSPREAD			
2	DNAT	DP-710	+00:30:50	872331	> R:725 EDP_PWMGEN_BIT_COUNT_MIN L=2	Bit	Name	Value	Description	
3	DNAT	DP-710	+00:30:50	872403	< ACK 02 0C					÷
4	DNAT	DP-710	+00:30:50.	872482	> R:2E RX_ALPM_CAPABILITIES L=1	0	MAX_DOWNSPREAD	1	Up to 0.5%	
5	DNAT	DP-710	+00:30:50.	872554	< ACK 03	2	STREAM REGEN STRIUS_CAP	n(0)	Reserved	
6	DNAT	DP-710	+00:30:50	872624	> W:116 RX_ALPM_CONFIGURATION L=1 01	3		0	Reserved	
7	DNAT	DP-710	+00:30:50	872704	< ACK	4		0	Reserved	
в	DHDCP	DP-710	+00:30:50.	873436	> R:69493 RxStatus L=1	5		0	Reserved	
9	DHDCP	DP-710	+00:30:50	873509	< ACK 00	6	NO AUX HANDSHAKE LINK TRAINING	1 N(0)		
0	DPLT	DP-T10	+00:30:50	935325	> R:100 LINK_BW_SET L=2		TEAT OVERVELED	*(1)		
1	DPLT	DP-710	+00:30:50	935398	< ACK 1E 04	02204: N	IORP			
2	DNAT	DP-710	+00:30:51	030734	> R:200 SINK_COUNT L=6	Bit	Name	Value	Description	
3	DNAT	DP-710	+00:30:51.	.030807	< ACK 41 04 00 00 00 00	<				

Pixel Error Test for Cables and Distribution Devices

The M41d support a Pixel Error test (or a Pseudo-Random Noise tests for verifying cables and distribution

equipment, The test is run in a loopback configuration (not shown).





DISPLAY STREAM COMPRESSION (DSC) TESTING

DSC Analysis

The 980 DP 1.4 Video Generator / Analyzer module's DSC analysis feature enables developers to view the DisplayPort DSC related protocol elements such as the picture parameter set, end of chunk packets and compression flag settings in the VBID to ensure that these elements are occurring in the video stream and that they are occurring in the proper sequence. The DSC analysis feature also captures and decompresses the video frames enabling developers to examine them for compression artifacts. The Forward Error Correction (FEC) transport mechanism, which ensures reliable, error free video transport, can also be verified.



ACA DPCD Reads for DSC Capabilities

The 980 DP 1.4 Video Generator / Analyzer module's ACA utility provides a log of the Aux Channel transactions. The link training can be viewed as well as the DPCD register reads and writes involved in the setup and maintenance of Display Stream Compression (DSC) and Forward Error Correction (FEC).

Video Generation (DSC/FEC)

The module's DSC/FEC video generator feature enables display developers to transmit DSC/FEC streams. Users can selection from several test patterns and configure the colorimetry, bits per component, bits per pixel, line buffer bit depth and DSC slice configurations.



DSC Analysis showing Picture Parameter Set (PPS)



ACA showing DPCD reads for DSC capabilities

Ope	n Clos	se Export	Options	Filter	Find				
2) (D	SC_FEC] E	vents: 436 (19	37)						
L3	DNAT	DP-T30	+00:03:14	.822399	< ACK Start Time	<pre>: +00:03:14.815507</pre>			
4	DNAT	DP-T30	+00:03:14	.950100	> W:111 MSTM_CTRL L=1 00 Type	: Native			
15	DNAT	DP-T30	+00:03:14	.950181	< ACK O Direction	1: Reply			
16	DNAT	DP-R31	+00:03:14	.814726	> R:E TRAINING AUX RD_INTERVAL L=1	emiest			
17	DNAT	DP-R31	+00:03:14	.814799	< ACK 81	nguoso.			
18	DNAT	DP-R31	+00:03:14	.814870	> R:0 DFCD_REV L=1 00060; DSC SUPPO	JRT			
19	DNAT	DP-R31	+00:03:14	.814943	< ACK 14 Bit Name		Value	Description	
20	DNAT	DP-R31	+00:03:14	.815013	> R:2200 DP1.3_DPCD_REV L=16				
21	DNAT	DP-R31	+00:03:14	.815086	< ACK 14 1E C4 81 01 00 01 80 00 20 0 DSC Sup	port	Y(1)		
22	DNAT	DP-R31	+00:03:14	.815292	> R:90 FEC_CAPABILITY L=1 1 DSC Pas	s PPS Undate Cmn->Cmn	N(0)		
23	DNAT	DP-R31	+00:03:14	.815365	< ACK BF 3 Dynamic	2 PPS Update UnCmp->Cmp	N(0)		
4	DNAT	DP-R31	+00:03:14	.815434	> R:60 DSC SUPPORT L=15 4		0	Reserved	
:5	DNAT	DP-R31	+00:03:14	.815507	< ACK 01 21 03 7F FB 07 01 00 00 0F 5		0	Reserved	
6	DPLT	DP-R31	+00:03:14	.822172	> W:100 LINK_BW_SET L=1 1E		0	Reserved	
27	DPLT	DP-R31	+00:03:14	.822253	< ACK 7		0	Reserved	
8	DNAT	DP-R31	+00:03:14	.822318	> W:600 SINK_SET_POWER L=1 01 00061: DSC ALGOR	RITHM REVISION			
9	DNAT	DP-R31	+00:03:14	.822399	< ACK Bit Name		Value	Description	
0	DNAT	DP-R31	+00:03:14	.950100	> W:111 MSTM_CTRL L=1 00				÷
1	DNAT	DP-R31	+00:03:14	.950181	< ACK 3-0 Version	a Major	1		
2	DNAT	DP-T30	+00:03:15	.274150	> R:200 SINK_COUNT L=6 7-4 Version	1 Minor	2		
3	DNAT	DP-T30	+00:03:15	.274222	< ACK 41 00 02 00 80 02 00062: DSC RC BL	JFFER BLOCK SIZE			
4	DNAT	DP-T30	+00:03:15	.274397	> R:E TRAINING_AUX_RD_INTERVAL L=1 Bit Name		Value	Description	
15	DNAT	DP-T30	+00:03:15	.274470	< ACK 81				÷
6	DNAT	DP-T30	+00:03:15	.274578	> R:0 DPCD REV L=1 1-0 Block S	size	3	64KB	
37	DNAT	DP-T30	+00:03:15	.274651	< ACK 14 2		0	Reserved	
8	DNAT	DP-T30	+00:03:15	.274724	> R:2200 DP1.3_DPCD_REV L=16		ŏ	Reserved	
9	DNAT	DP-T30	+00:03:15	.274797	< ACK 14 1E C4 81 01 00 01 80 00 20 5		0	Reserved	
0	DNAT	DP-T30	+00:03:15	.275042	> R:90 FEC_CAPABILITY L=1 6		0	Reserved	
1	DNAT	DP-T30	+00:03:15	.275115	< ACK BF				
2	DNAT	DP-T30	+00.03.15	275182	> 8:60 DSC SUPPORT L=15	< ACK 01 21 03 7F FB 07	01 00	0.00 OF OF FE	

DSC / FEC Video Generation



Test Setup for Sink Test

DISPLAY STREAM COMPRESSION (DSC) COMPLIANCE

DSC Compliance

The 980 DSC source and sink compliance tests are ideal for pre-testing your DisplayPort source, sink or repeater product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged during the test to help diagnose the cause of compliance test failures. (Refer to the test setups on the previous page.)

DSC Source Tests

S DP 1.4a DSC Source CT R1.1	-		×
Instrument: AL_M41d [10.30.196.30] - Connect Cards			
CDF Entry Test Selection Test Options / Pr	eview		
Select All 🗹 🕱 Count Options	EX	ECUTE	TESTS
~ Dsc			
4.6.1.1: DSC enable sequence verification		1	×
 4.6.1.2: DSC PPS block prediction flag verification 		1	1
4.6.1.3: DSC PPS convert RGB flag verification		1	1
4.6.1.4: DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification		1	1
4.6.1.5: DSC PPS Simple 4:2:2 flag verification		1	×
4.6.1.6: DSC PPS Native 4:2:2 flag verification		1	1
4.6.1.7: DSC PPS Native 4:2:0 flag verification		1	1
4.6.1.8: DSC PPS convert RGB flag verification for DSC Algorithm revision 1.1		1	1
4.6.1.9: DSC PPS (YCbCr 4:4:4 convert RGB = 0) flag verification for DSC Algorithm revision 1	.1	1	×

DSC Sink Tests

일 DP	1.4a DSC Sink CT R1.1	-		×
Inst	rument: Al_M41d [10.30.196.30] - Connect Cards			
	CDF Entry Test Selection Test Options / Prev	iew		ſ
Selec	at All 🛷 🗰 Count Options	EXEC	JTE TEST	s
~ [Dsc			
>	5.6.1.1: DSC capability verification	1	1	
>	5.6.1.2: DSC RGB color depth test	1	1	
>	5.6.1.3: DSC RGB Block prediction test	1	~	
>	5.6.1.4: DSC RGB bits-per-pixel test	1	×	
>	5.6.1.5: DSC RGB slice test	1	1	
>	5.6.1.6: DSC RGB lanes test	1	1	
>	5.6.1.7: DSC YCbCr 4:4:4 color depth test	1	1	
>	5.6.1.8: DSC YCbCr 4:4:4 Block prediction test	1	×	
>	5.6.1.9: DSC YCbCr 4:4:4 bits-per-pixel test	1	1	
>	5.6.1.10: DSC YCbCr 4:4:4 slice test	1	1	
>	5.6.1.11: DSC YCbCr 4:4:4 lanes test	1	1	
>	5.6.1.12: DSC Simple 4:2:2 color depth test	1	1	
>	5.6.1.13: DSC Simple 4:2:2 Block prediction test	1	1	
>	5.6.1.14: DSC Simple 4:2:2 bits-per-pixel test	1	1	
>	5.6.1.15: DSC Simple 4:2:2 slice test	1	1	
>	5.6.1.16: DSC Simple 4:2:2 lanes test	1	1	
>	5.6.1.17: DSC Native 4:2:2 color depth test	1	1	
>	5.6.1.18: DSC Native 4:2:2 Block prediction test	1	1	
>	5.6.1.19: DSC Native 4:2:2 bits-per-pixel-test	1	×	
>	5.6.1.20: DSC Native 4:2:2 slice test	1	1	
>	5.6.1.21: DSC Native 4:2:2 lanes test	1	×	

DSC Sink Tests – Test Results

Compliance Test Results Viewer	
DP 1.4a DSC Sink (R1.0) Compliance Test	Results
esults Name: DUT1_DSC_TEST_ALL Manufacturer:	HTML Re
Date Lested: October 30, 2019 5:53 PM Model Name:	
verall Status: CIS R1.0 - Fail Port Tested: 1	
Test Results	
Test Name / Details	Status
5.6.1.4: DSC RGB bits-per-pixel test	Pass
5.6.1.5: DSC RGB slice test	Pass
5.6.1.6: DSC RGB lanes test	Pass
5.6.1.7: DSC YCDCr 4:4:4 Color depth test	Pass
E 5.6.1.8: DSC YCDCr 4:4:4 Block prediction test	Dass
5.6.1.10: DSC VCbCr 4:4:4 bits-per-pixer test	Pass
5.6.1.11: DSC YCCCr 4:4:4 lanes test	Pass
5.6.1.12: DSC Simple 4:2:2 color depth test	Pass
5.6.1.13: DSC Simple 4:2:2 Block prediction test	Pass
5.6.1.14: DSC Simple 4:2:2 bits-per-pixel test	Pass
5.6.1.15: DSC Simple 4:2:2 slice test	Pass
5.6.1.16: DSC Simple 4:2:2 lanes test	Pass
E 5.6.1.17: DSC Native 4:2:2 color depth test	Pass
5.6.1.18: DSC Native 4:2:2 Block prediction test	Pass
5.6.1.19: DSC Native 4:2:2 bits-per-pixel-test	Pass
5.6.1.20: DSC Native 4:2:2 slice test	Pass
5.6.1.21: DSC Native 4:2:2 lanes test	Pass
5.6.1.22: DSC Native 4:2:0 color depth test	Fall
5.6.1.23: DSC Native 4:2:0 Block prediction test	Pall
5.6.1.24: DSC Native 4:2:0 bits-per-pixel test	Dass
5.6.1.25: DSC Native 4:2:0 Since test	Pass
5 6 2 1: DSC Height test	Fail
5.6.2.2: DSC Padding test	Pass
5.6.2.3: DSC RGB min and max bits-per-pixel test	Pass
▲	Pass
A	and lane count Pass
HPD is asserted	
 Reference Source receives AUX_ACK at 1 attempts 	
 Reference Source receives AUX ACK from either write reque 	st
AUX Read UX2201 (MAX_LINK_RATE) = Ux1e	
ANA Read 0x2202 (MAA_LANS_COUNT) = 0x04	
A Design of the second of	PC check on V Pass
03: For Timing 1920x1080p@60Hz bpc 8 hpp 24.000	CRC check or Pass
♦ 04: For Timing 1920x1080pe60Hz bpc 10 hpp 8.000	CRC check or Pass
▷) CRC check or Pass
▷	CRC check or Pass
▷	CRC check or Pass
5.6.2.4: DSC YCbCr 4:4:4 min and max bits-per-pixel	test Pass
Den ACA Data	
nstrument: PG980B [10.30.196.27]	Continue Test Execut

DSC Source Tests - Test Results

DP 144 Source (Core B.C.O) Complement Park Results Dete Teack innung2, 20105 AM Model Name: Dete Teack innung2, 20105 AM Model Name: P Teat Base / Details Test Roots Image: Test Roots Test Roots P Test Base / Details Status Image: Test Roots Feas Image: Test Roots Feas <td< th=""><th></th><th></th><th></th></td<>			
Readt Name: TWN-05:2,5mple Manufacture: Noids DP/ANT/HBS Det Fred: Name: 2,203:03:3M Model Name: Det Fred: Name: 2,203:03:3M For Tests 1 Det Fred: Name: 2,203:03:3M Model Name: Part: Name: 7, Det Name: 2,203:03:3M Model Name: Det Fred: Name: 2,203:03:3M Model Name: Part: Name: 7, Det Name: 2,203:03:03:03:03:03:03:03:03:03:03:03:03:0	DP 1.4a Sour	ce (Core R1.0) Compliance Test Results	
Date Tends: January 23, 203 1005 AM Model Name: Derail Status: Store Status: Status	Results Name: TENV-DSC_2_Sample	Manufacturer: Nividia DP/MST/HBR3	HTML Report
Devend Status Fort Texts 1 Text Name / Details Status Text Name / Details Status Text Name / Details Status Text Name / Details Status Text Name / Details Status Status S	Date Tested: January 23, 2019 10:55 AM	Model Name:	
Test Rame / Details Test Rame / Details Provide the set of the second	Overall Status: CTS Core R1.0 - Pass	Port Tested: 1	
<pre>> Text Name / Details</pre>		Test Results	
 ↓ Her Gi: ↓ Goit: [1] DSC Test 1 Lane count = 2 and lane rate = 8.10 ↓ Source DUT reads FEC CAMANILITY register GasOb. ↓ ↓ C. 12: DSC FES block prediction flag verification ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓	Test Name / Details		Status ^
 Gl: [1] DBC Test 1 lane count = 2 and lane rate = 8.10 Source DUT sets FEC CARADILITY register Cost CONTIGURATION register. Source DUT sets FEC MARKING to The Control of the Con	A A Iter 01:		Pass
<pre>source DUT reads FEC CAABAILITY register Qs90 source DUT reads FEC CAABAILITY register Cs90 source DUT reads FEC CAAB</pre>	▲	and lane rate = 8.10	Pass
 Source DUT sets FEC (READY before link training to FEC CONTIGURATION register. P. 4. 6.1.2: DSC FPS block prediction flag verification P. 4. 6.1.2: DSC FPS block prediction flag verification P. 4. 6.1.2: DSC FPS block prediction flag verification P. 4. 6.1.2: DSC FPS block prediction flag verification P. 4. 6.1.2: DSC FPS block prediction flag verification P. 4. 6.1.3: DSC FPS convert RGB flag verification P. 4. 6.1.3: DSC FPS convert RGB flag verification P. 4. 6.1.3: DSC FPS convert RGB flag verification P. 4. 6.1.3: DSC FPS convert RGB flag verification P. 4. 6.1.3: DSC FPS convert RGB flag verification P. 4. 6.1.4: DSC FPS convert RGB flag verification P. 4. 6.1.4: DSC FPS convert RGB flag verification P. 4. 6.1.4: DSC FPS convert RGB flag verification P. 4. 6.1.4: DSC FPS convert RGB flag verification P. 4. 6.1.4: DSC FPS convert RGB flag verification P. 4. 6.1.4: DSC FPS reg and color depth bits-per-component 10 P. 6.1: (1) DSC Test 2 for lane count = 2 and lane rate = 8.10 P. 6.1: (1) DSC FPS (PCbCr 4.4:4 convert RGB = 0) flag verification P. 6.1: (1) DSC Fest 2 for lane count = 2 and lane rate = 8.10 P. 6.1: (1) DSC Fest 2 for lane count = 2 and lane rate = 8.10 P. 6.1: (1) DSC Fest 2 for lane count = 2 and lane rate = 8.10 P. 6.1: (1) DSC Fest 2 for lane count = 2 and lane rate = 8.10 P. 6.1: (1) DSC Fest 2 for lane count = 2 and lane rate = 8.10 P. 6.1: (1) DSC Fest 2 for lane count = 2 and lane rate = 8.10 P. 6.1: (1) DSC Fest 2 for lane count = 2 and lane rate = 8.10 P. 6.1: (1) DSC Fest 2 for lane count = 2 and lane rate = 8.10 P. 6.1: (1) DSC Fest 2 for lane count = 2 and lane rate = 8.10 P. 6.1: (1) DSC Fest 2 for lane count =	Source DUT reads FEC CAPABILITY register	0x90h.	
 PFS validation successful. No error found. 4.6.1.2.1 DSC PFS holock prediction flag verification Pass Point PFS validation successful. No error found. Source DUT reads FFC CANANILITY register 0x50h. Source DUT sends FFS validation successful. No error found. Refrence sink does not support INGE. Source DUT sends FFS with block prediction disable. If DEC Test 2 for lane count = 2 and lane rate = 6.10 Pass O 11: [1] DSC Test 2 for lane count = 2 and lane rate = 6.10 Pass PFS validation successful. No error found. Refrece sink only supports RNGE. Source DUT sends FFS with covert_rop set. Source DUT sends PIs and color depth bits-per-component 12 O 01: [1] DSC Test 2 for lane count = 2 and lane rate = 6.10 O 03: [3] For XGE and color depth bits-per-component 12 O 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 Source DUT sends FEC CANABILITY register tox50h. Sourc	Source DUT sets FEC_READY before link tr	aining to FEC_CONFIGURATION register.	
<pre></pre>	PPS validation successful. No error four	nd.	
 ↓ Let C1: ↓ O 11: [] DSC Test 2 for lane count = 2 and lane rate = 8.10 ↓ Source DUT reads FEC CAABULITY register 0x500. ↓ Source DUT reads FEC CAABULITY register 0x500. ↓ Source DUT reads FEC CAABULITY register 0x500. ↓ ♥ Termone Sink does not support Dick the prediction. Source DUT sends PFS with block prediction disable. ♥ FFS wildedino successful. No error found. ▶ ■ Reference Sink does not support Dick prediction. Source DUT sends PFS with block prediction disable. ♥ ● 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ ● 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ ● 01: [2] For RGB and color depth bits-per-component 8 ♥ ■ PFS wildedino successful. No error found. ■ Reference Sink Only supports NGS. Source DUT sends PFS with covert_rop set. ♥ 503: [3] For RGB and color depth bits-per-component 12 ♥ 031: [4] For RGB and color depth bits-per-component 12 ♥ 031: [4] For RGB and color depth bits-per-component 12 ♥ 041: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 051: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 051: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 051: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 051: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 051: [2] For YCbCr 4:4:4 and color depth bits-per-component 12 ♥ 051: [3] For YCbCr 4:4:4 and color depth bits-per-component 12 ♥ 051: [3] For YCbCr 4:4:4 and color depth bits-per-component 12 ♥ 051: [3] For YCbCr 4:4:4 and color depth bits-per-component 12 ♥ 051: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 051: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 051: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 051: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 05	4 .6.1.2: DSC PPS block prediction flag	g verification	Pass
 ← 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 Fource DUT reads FEC CAABUITY register DSOB. Source DUT sets FEC READY Defore link training to FEC_CONFIGURATION register. FF wildation ascessful. No error found. A.6.1.3: DSC PFS convert ROB flag verification Fource DUT sets FEC READY Defore link training to FEC_CONFIGURATION register. FF wildation ascessful. No error found. Fource DUT sets FEC READY Defore link training to FEC_CONFIGURATION register. Fource DUT sets FEC READY Defore link training to FEC_CONFIGURATION register. Fource DUT sends Dita-per-Component 8 FOT ROB and color depth Dita-per-component 10 Fource DUT sends Dita-per Component 10 Fource DUT sends FEC CAABUITY register DSOB. Fource DUT sends FEC CANDITY register DSOB. Source DUT sends FEC READY before link training to FEC CONFIDURATIO	4 😑 Iter 01:		Pass
 Source DUT reads FEC CAABAILITY register Dx900. Source DUT sends FEC CAABAILITY register Dx900. Source DUT sends FEC CAABAILITY register Dx900. FFS validation successful. No error found. Betremoe sink does not support Dlock prediction. Source DUT sends PFS with block prediction disable. A 6.1.3: DSC DPS convert ROB flag verification FFS validation successful. No error found. FFS validation successful. Yes on the successful value of the succe	▲	= 2 and lane rate = 8.10	Pass
 Source DUT sets FPC READY before link training to FPC CONFIDENTION register. PFF vilidation secossful. No error found. Refrence sink does not support block prediction. Source DUT sends FPS with block prediction disable. A. 6.1.3: DSC PPS convert ROB Flag verification PO 1: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 PO 2: [2] For RGB and color depth blis-per-component 8 PO 1: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 PO 2: [2] For RGB and color depth blis-per-component 8 PO 1: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 PO 2: [2] For RGB and color depth blis-per-component 10 PO 3: [3] FOR RGB and color depth blis-per-component 12 PO 4: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 PO 5: [3] FOR RGB and color depth blis-per-component 12 PO 4: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 PO 5: [3] FOR RGB and color depth blis-per-component 12 PA 5: [3] FOR YCBCR 4:4:4 and color depth blis-per-component 12 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 12 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 10 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 10 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 10 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 10 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 10 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 10 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 10 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 10 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 12 PA 5: [3] FOR YCBCR 4:4:4: and color depth blis-per-component 12	 Source DUT reads FEC CAPABILITY register 	0x90h.	
 #PF validation successful. No error found. Betrome sink does not support Dick prediction. Source DT sends PFS with block prediction disable. *** Latence sink does not support Dick prediction. Source DT sends PFS with block prediction disable. **** Latence sink doi: ************************************	 Source DUT sets FEC_READY before link tr 	raining to FEC_CONFIGURATION register.	
<pre>* Refremce sink does not support block prediction. Source DUT sends PFS with block prediction disable. * 4.6.1.3: DSC PFS convert ROB Hag verification PFS with block prediction disable. * 0 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 * 0 02: [2] For ROB and color depth blis-per-component 8 * 0 02: [2] For ROB and color depth blis-per-component 10 * 0 02: [3] FOR ROB and color depth blis-per-component 10 * 0 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 * 0 02: [3] FOR ROB and color depth blis-per-component 10 * 0 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 * 0 01: [1] DSC T</pre>	 PPS validation successful. No error four 	nd.	
<pre>A _ to.1.3; DSC DPS convert NoB flag Verification</pre>	 Refrence sink does not support block pre 	diction. Source DUT sends PPS with block prediction disable.	Dees
<pre>> O 1: (1) DSC rest 2 for lane count = 2 and lane rate = 8.10 > O 1: (1) DSC rest 2 for lane count = 2 and lane rate = 8.10 > Poss > O 2: (2) Por RCB and color depth bits-per-component 8 > Surre DT mends hits-par-Component 5 > O 0: (3) For RCB and color depth hits-per-component 10 > O 0: (4) For RCB and color depth hits-per-component 12 > O 0: (1) ESC rest 2 for lane count = 2 and lane rate = 8.10 > O 0: (2) For YCHC 4:4:4 convert RCB = 0) flag verification > Surce DT sets FEC CANADILITY register X000. > Source DT sets FEC CANADILITY register X000. > O 0: (3) For YCHC 4:4:4 and color depth hits-per-component 10 > O 0: (3) For YCHC 4:4:4 and color depth hits-per-component 10 > O 0: (3) For YCHC 4:4:4 and color depth hits-per-component 10 > O 0: (3) For YCHC 4:4:4 and color depth hits-per-component 10 > O 0: (3) For YCHC 4:4:4 and color depth hits-per-component 10 > O 0: (3) For YCHC 4:4:4 and color depth hits-per-component 10 > O 0: (3) For YCHC 4:4:4 and color depth hits-per-component 10 > O 0: (3) For YCHC 4:4:4 and color depth hits-per-component 10 > O 0: (3) For YCHC 4:4:4 and color depth hits-per-component 10 > O 0: (3) For YCHC 4:4:4 and color depth hits-per-component 10 > O 0: (1) DSC Test 2 for lane count = 2 and lane rate = 6.10 > O 0: (1) DSC Test 2 for lane count = 2 and lane rate = 6.10 > O 0: (1) DSC Test 2 for lane count = 2 and lane rate = 6.10 > O 0: (3) For Simple 4:2:2 and color depth hits-per-component 8 > O 0: (3) For Simple 4:2:2 and color depth hits-per-component 12 > O 0: (3) For Simple 4:2:2 and color depth hits-per-component 12 > O 0: (4) For Simple 4:2:2 and color depth hits-per-component 12 > O 0: (4) For Simple 4:2:2 and color depth hits-per-component 12 > O 0: (4) For Simple 4:2:2 and color depth hits-per-component 12 > O 0: (4) For Simple 4:2:2 and color depth hits-per-component 12 > O 0: (4) For Simple 4</pre>	4 0 4.6.1.3: DSC PPS Convert RGB flag Ver	Irication and a second s	Pass
<pre>v 01: [1] USC 1885 2 and color depth bits-per-component 8 v 02: [2] Por RGB and color depth bits-per-component 8 v 03: [3] For RGB and color depth bits-per-component 10 v 03: [3] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For RGB and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For IChCr 4:4:4 and color depth bits-per-component 12 v 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 v 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 v 04: [4] For Simple 4:2:2 and</pre>		- 0	Dana
<pre> * PF* validation successful. No error found. * Northermos ink only supports RGS. Source DUT sends PFS with covert_rgb set. * Source DUT sends bits-per-Component 10 * Of: [3] FOR RGS and color depth bits-per-component 12 * Ods: * Ods: [4] FOR RGS end color depth bits-per-component 12 * Ods: * Ods: [1] FOR YES CONSTULY register Component 12 * Ods: * Ods: [2] FOR YCHCP 4:4:4 convert RGB = 0) flag verification * Source DUT sends PEC CANADILITY register Component 12 * Ods: * Ods: [2] FOR YCHCP 4:4:4 and color depth bits-per-component 12 * Ods: * Source DUT sends PEC CANADILITY register Component 12 * Ods: * Source DUT sends PEC CANADILITY register Component 12 * Ods: * Source DUT sends PEC CANADILITY register Component 12 * Ods: * Source DUT sends PEC CANADILITY register Component 12 * Ods: * Source DUT sends PEC CANADILITY register Component 12 * Ods: * Ods: * Source DUT sends PEC CANADILITY register Component 10 * Pess * Ods: * Ods:</pre>	↓ 01: [1] DSC Test 2 For Take count	= 2 and lane rate = 0.10	Decc
 Bartrence sith only supports SGR. Source DUT sends PFS with covert_rdb set. Source DUT sends bits-per-Component 5. User indicated that image looks ok and distortion free. Od: [4] FDS RGB and color depth bits-per-component 12 A. 6.1.4.1 ADGC PPS NGDC 44:4 and color depth bits-per-component 12 Basic DUT reds FEC CAMANLINT register 0x900. Source DUT reds FEC CAMANLINT register 0x9000. Source DUT reds FEC CAMANLINT register 0x900. Source DUT reds FEC CAMANLINT register 0x9000. Source DUT reds FEC CAMANLINT register 0x90000000. Source DUT reds F	PPS validation successful. No error four	ad.	1055
 Source DUT sends bits-per-Component 8. ♥ Got indicated that image looks and disortion free. ♥ 03: [3] For RGE and color depth bits-per-component 10 ₽ 04: [4] For RGE and color depth bits-per-component 12 ₽ 4. (4. 6.1. 4: DSC DPS (YChCF 4:4:4 convert RGB = 0) flag verification ₽ 5 source DUT seads FEC CARADILITY register CASOD. ♥ 5 source DUT seads FEC CARADILITY register CASOD. ♥ 5 source DUT seads FEC CARADILITY register CASOD. ♥ 6 01: [3] For YChCF 4:4:4 and color depth bits-per-component 8 ₽ 03: [3] For YChCF 4:4:4 and color depth bits-per-component 10 ₽ 20: [3] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 03: [3] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 03: [3] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 04: [4] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 05: [3] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 05: [3] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 04: [4] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 04: [4] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 04: [4] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 04: [4] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 04: [4] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 04: [4] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 05: [3] For YChCF 4:4:4 and color depth bits-per-component 12 ₽ 05: [4] For Simple 4:2:2 and color depth bits-per-component 12 ₽ 05: [3] For Simple 4:2:2 and color depth bits-per-component 10 ₽ 05: [3] For Simple 4:2:2 and color depth bits-per-component 10 ₽ 05: [3] For Simple 4:2:2 and color depth bits-per-component 12 ₽ 03: [3] For Simple 4:2:2	Refrence sink only supports RGB. Source	DUT sends PPS with covert rob set.	
 User indicatied that image looks ok and distortion free. ♥ 03: [3] For RGB and color depth bits-per-component 10 ♥ 04: [4] For RGB and color depth bits-per-component 12 ♥ 04: [4] For RGB and color depth bits-per-component 12 ♥ 04: [4] For RGB and color depth bits-per-component 12 ♥ 04: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 03: [2] For YCbCT 4::4: and color depth bits-per-component 10 ♥ 04: [3] For YCbCT 4::4: and color depth bits-per-component 10 ♥ 04: [3] For YCbCT 4::4: and color depth bits-per-component 10 ♥ 04: [3] For YCbCT 4::4: and color depth bits-per-component 10 ♥ 04: [4] For YCbCT 4::4: and color depth bits-per-component 10 ♥ 04: [4] For YCbCT 4::4: and color depth bits-per-component 10 ♥ 04: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 04: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 04: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 04: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 04: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 04: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 ♥ 03: [3] For Simple 4:2:2 and color depth bits-per-component 8 ♥ 03: [3] For Simple 4:2:2 and color depth bits-per-component 10 ♥ 03: [3] For Simple 4:2:2 and color depth bits-per-component 10 ♥ 03: [3] For Simple 4:2:2 and color depth bits-per-component 10 ♥ 03: [3] For Simple 4:2:2 and color depth bits-per-component 10 ♥ 03: [3] For Simple 4:2:2 and color depth bits-per-component 10 ♥ 04: [4] For Simple 4:2:2 and color depth bits-per-component 10 ♥ 04: [4] For Simple 4:2:2 and color depth bits-per-component 10 ♥ 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 ♥ 04:	Source DUT sends bits-per-Component 8.		
<pre>> ● 03: [3] FOR RGE and color depth bits-per-component 10 Pass > ● 04: [4] FOR RGE and color depth bits-per-component 12 Pass > ● 14: [4] FOR RGE PS (YChCF 4:4:4 convert RGB = 0) flag verification Pass > ● 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 > ● 01: [2] FOR YChCF 4:4:4 and color depth bits-per-component 1 Pass > ● 02: [2] FOR YChCF 4:4:4 and color depth bits-per-component 1 Pass > ● 03: [3] FOR YChCF 4:4:4 and color depth bits-per-component 1 Pass > ● 03: [3] FOR YChCF 4:4:4 and color depth bits-per-component 1 Pass > ● 03: [3] FOR YChCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [4] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 2 Pass > ● 04: [2] FOR YCHCF 4:4:4 and color depth bits-per-component 2 Pass > ● 05: [3] FOR YCHCF 4:4:4 and color depth bits-per-component 2 Pass > ● 04: [4] FOR YCHCF 4:4:4 and color depth bits-per-component 2 Pass > ● 04: [4] FOR YCHCF 4:4:4 and color depth bits-per-component 2 Pass > ● 04: [3] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [4] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [4] FOR YCHCF 4:4:4 and color depth bits-per-component 1 Pass > ● 04: [4] FOR YCHCF 4:4</pre>	• User indicatied that image looks ok and	distortion free.	
<pre>> 0 04; [4] FOR RGB and color depth hits-per-component 12 F005 (4.6.1.4.1 DSC PPS (YChCr 4:4:4 and convert RGB = 0) flag verification F335 (11) DSC Test 2 for lane count = 2 and lane rate = 8.10 F335 (12) DSC Test 2 for lane count = 2 and lane rate = 8.10 F335 (13) FOR YChCr 4:4:4 and color depth hits-per-component 10 F335 (14) FOR YChCr 4:4:4 and color depth hits-per-component 10 F335 (15) FOR YChCr 4:4:4 and color depth hits-per-component 10 F335 (14) FOR YChCr 4:4:4 and color depth hits-per-component 10 F335 (15) FOR YChCr 4:4:4 and color depth hits-per-component 10 F335 (15) FOR YChCr 4:4:4 and color depth hits-per-component 10 F335 (15) FOR YChCr 4:4:4 and color depth hits-per-component 10 F335 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR PS Simple 4:2:2 flag verification F355 (14) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 1 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 2 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 2 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 2 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 2 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 2 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 and color depth hits-per-component 12 F355 (15) FOR YChCr 4:4:4 color depth hits-per-component 12 F355 F35 F35 F35 F35 F35 F35 F35 F35 F3</pre>	>	lts-per-component 10	Pass
<pre></pre>	>	its-per-component 12	Pass
<pre>A ● Cler DI: PRASE</pre>	4 🗄 4.6.1.4: DSC PPS (YCbCr 4:4:4 convert	RGB = 0) flag verification	Pass
<pre></pre>	4 😝 Iter 01:		Pass
 Source DUT reads FEC CAABAILITY register 0x500. Source DUT reads FEC CAABAILITY register 0x500. Source DUT sets FEC CAABAILITY register 0x500. C 21 [2] For YCbCT 4:4:4 and color depth bits-per-component 8 Pass O 3: [3] For YCbCT 4:4:4 and color depth bits-per-component 10 Pass O 4: [4] For YCbCT 4:4:4 and color depth bits-per-component 10 Pass O 4: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 Pass O 0: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 Pass O 0: [2] For Simple 4:2:2 and color depth bits-per-component 8 Pass Pass O 1: [3] For YCbCT 4:4:4 and color depth bits-per-component 8 Pass O 0: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 Pass O 0: [2] For Simple 4:2:2 and color depth bits-per-component 8 Pass O 0: [3] For Simple 4:2:2 and color depth bits-per-component 1 Pass O 0: [3] For Simple 4:2:2 and color depth bits-per-component 10 Pass O 0: [3] For Simple 4:2:2 and color depth bits-per-component 10 Pass O 0: [3] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 0: [3] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 0: [5] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 0: [5] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 0: [5] For Simple 4:2:2 and color depth bits-per-component 12 Pass C 4.6.1.6: DSC PPS Native 4:2:2 flag vortfloation Skilped • V 00: [6] For Simple [6] For Simple 4:2:2 and color depth bits-per-component 12 Pass Pass [6] [6] [6] [6] [6] [6] [6] [6] [6]	▲	= 2 and lane rate = 8.10	Pass
<pre>source DUT sets FRC READY before link training to FRC_CONFIGNATION register.</pre>	 Source DUT reads FEC CAPABILITY register 	0x90h.	
 > © 02: [2] For YCbCr 4:4:4 and color depth bits-per-component 8 PO 33: [3] For YCbCr 4:4:4 and color depth bits-per-component 10 Poss > © 04: [4] For YCbCr 4:4:4 and color depth bits-per-component 12 Pass > © 04: [4] For YCbCr 4:4:4 and color depth bits-per-component 12 Pass > © 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 Pass > © 01: [1] DSC Test 2 for lane count = 2 and lane rate = 6.10 Pass > © 02: [2] For Simple 4:2:2 and color depth bits-per-component 8 Pass > © 01: [3] For Simple 4:2:2 and color depth bits-per-component 8 Pass > © 01: [3] For Simple 4:2:2 and color depth bits-per-component 10 Pass > © 01: [3] For Simple 4:2:2 and color depth bits-per-component 10 Pass > © 01: [3] For Simple 4:2:2 and color depth bits-per-component 10 Pass > © 01: [4] For Simple 4:2:2 and color depth bits-per-component 12 > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > Pass > © 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 > Pass<!--</td--><td> Source DUT sets FEC_READY before link tr </td><td>aining to FEC_CONFIGURATION register.</td><td></td>	 Source DUT sets FEC_READY before link tr 	aining to FEC_CONFIGURATION register.	
<pre>>> 03: [3] For YCbCr 4:4:4 and color depth bits-per-component 10 >> 04: [4] For YCbCr 4:4:4 and color depth bits-per-component 12 Plass >> 04: [4] For YCbCr 4:4:4 and color depth bits-per-component 12 Plass >> 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 >> 01: [2] For Simple 4:2:2 and color depth bits-per-component 8 >> 02: [2] For Simple 4:2:2 and color depth bits-per-component 8 >> 03: [3] For Simple 4:2:2 and color depth bits-per-component 8 >> 03: [3] For Simple 4:2:2 and color depth bits-per-component 10 >> 03: [3] For Simple 4:2:2 and color depth bits-per-component 10 >> 03: [3] For Simple 4:2:2 and color depth bits-per-component 10 >> 03: [3] For Simple 4:2:2 and color depth bits-per-component 10 >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Plass >> 04: [4] For S</pre>	▷	depth bits-per-component 8	Pass
<pre>>> 0 04: [4] For YCDCP 44:43 and color depth bits-per-component 12 PASS >> 0 04: [4] For YCDCP 44:43 and color depth bits-per-component 12 PASS >> 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 Pass >> 01: [1] DSC Test 2 for lane count = 2 and lane rate = 8.10 Pass >> 02: [2] For Simple 4:2:2 and color depth bits-per-component 8 Pass >> 8 Refrence sink only supports RDB and Simple 4:2:2. Source DUT sends PFS vith simple 4:22 set. >> 02: [3] For Simple 4:2:2 and color depth bits-per-component 10 Pass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 10 Pass >> 04: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass >> 04: [4] For Simple 4:2:2 flag verification Skipped >> 06: [4] For Simple 4:2:2 flag verification Pass >> 06: [4] For Simple 4:2:2 flag verification Pass Pass >> 06: [4] For Simple 4:2:2 flag verification Pass Pass Pass >> 06: [4] For Simple 4:2:2 flag verification Pass Pas</pre>	▷	depth bits-per-component 10	Pass
<pre> troils: Discrept of provide the second s</pre>	▷ ⊕ 04: [4] For YCbCr 4:4:4 and color	depth bits-per-component 12	Pass
Vort GL:	A E 4.6.1.5: DSC PPS Simple 4:2:2 flag ver	rification	Pass
<pre>> O(2; [1]) EDG 185L7 Color Lattle Color > & fill Life Table Table (0; [2]) For Simple 4:2:2 and color depth bits-per-component 8</pre>	Alt (11 DEC Test 2 fem lane sount	- 2 and long mate - 8 10	Dace
PEP validation successful. No error found. A per validation successful. No error found. A per validation successful. No error found. A per validation successful. No error found. Source DUT sends PEP validation free. Source DUT sends PEP validation free. O d: [4] For Simple 4:2:2 and color depth bits-per-component 10 Pass O d: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass A c6.1.c6 DSC PEP Native 4:2:2 flag varification Pore ACADs. 45.1105C endbe sequence verification Inturnet SS008[0.3195.39]	▲ 02: [2] For Simple 4:2:2 and color	- 2 and fame face - 0.10	Pass
Befrence sink only supports BOB and Simple 4:2:2. Surce DUT sends PPS with simple_422 set. Surce DUT sends bits-per-Component 0. Surce DUT sends bits-per-Component 0. Post Out (4) For Simple 4:2:2 and color depth bits-per-component 12 Post Post Post Skipped - OpenACADB Skipped Intument [SSB08[10.3195.39] P Context testSection	 PPS validation successful. No error four 	d.	
Source DUT sends bits-per-Component 8. User indicatied that image looks ok and discrition free. User indicated that image looks ok and discrition free. O 3: [3] For Simple 4:2:2 and color depth bits-per-component 10 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass O 4: [4] For Simple 4:2:2 and color depth bits-per-component 12 O 4: [4] For Simple 4:2:2 and color 4: [4] For Simple 4	Refrence sink only supports RGB and Simp	ble 4:2:2. Source DUT sends PPS with simple 422 set.	
User indicated that image looks ok and distortion free. Set of the image looks ok and distortion free. Set of the image looks ok and distortion free. Set of the image looks ok and color depth bits-per-component 10 Pass Set of the image looks of the image looks ok and color depth bits-per-component 12 Pass Set of the image looks of the image looks ok and color depth bits-per-component 12 Pass Set of the image looks ok and color depth bits-per-component 12 Pass Set of the image looks ok and color depth bits-per-component 12 Pass Set of the image looks ok and color depth bits-per-component 12 Pass Poss Set of the image looks of the image looks ok and color depth bits-per-component 12 Pass Poss Set of the image looks of the	 Source DUT sends bits-per-Component 8. 		
>> 0.3: [3] For Simple 4:2:2 and color depth bits-per-component 10 Pass >> 0.4: [4] For Simple 4:2:2 and color depth bits-per-component 12 Pass > 1.4: [6] Color Simple 4:2:2 flag vorification Skipped > 0.4: [4] For Simple 4:2:2 flag vorification Skipped > 0.4: [6] Control to Color PB Native 4:2:2 flag vorification Skipped > 0.4: [6] Control to Color PB Native 4:2:2 flag vorification For the control to Control to Color PB Native 4:2:2 flag vorification Instrument [55008 [10.3:19:39] • • Control to the color	• User indicatied that image looks ok and	distortion free.	
	>	r depth bits-per-component 10	Pass
> ■ 4.6.1.6: DSC PPS Native 4:2:2 flag verification Skipped □P Open ACA Data 4.511:05C enable sequence wellfaction Instrument [558088 [10.30:196:39] ▶ Centinue Test Execution ▶ Centinue Test Execution ▶ Centinue Test Execution ▶ Centinue Test Execution ▶ Centinue Test Execution 	Ø 04: [4] For Simple 4:2:2 and color	r depth bits-per-component 12	Pass
Gip Open ACA Data 45.11: DSC enable sequence welfication Instrument [SS008 [(0.3):195.39]	B 4.6.1.6: DSC PPS Native 4:2:2 flag ver Second State Seco	rification	Skipped -
Instrument SS8808 [10.30.196.39]	Den ACA Data 4.6.1.1: DSC enable sequence verification		
Instrument: [\$5980B [10.30.196.39]			1
	Instrument: [SS980B [10.30.196.39]	▼ ► Co	ntinue Test Execution
K Close			X Close

DP 1.4 LINK LAYER SOURCE COMPLIANCE

Source Link Layer Compliance Approved!

The 980 DP source HBR3 link layer compliance tests are approved by VESA and are ideal for self-testing or pretesting your HBR3-capable DisplayPort 1.4 source product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests (below right) enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. The link layer compliance test suite now includes tests for forward error correction (FEC). You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures (below).



DP Aux Channel Traces – From LLC Test

000	n Close	e Diana	Ontingo	Citrie .	Find					
ope	n Clos	e Export	Options	Filler	Find					
A IA	DA14_3_1_	TU_U1] Events	200 08:25	002422	Lenge	120	Phane Mines 100.00.02 010965			
-	DATA	DP-RJ1	+00.00.25	000404	N AND	1	Turne: Native			
	DRAT	DP-RSL	+00:08:25	972404	A R.R. TRAINING AUX RD INTERVAL DAI		Direction: Reply			
	DBAT	DP-RSI	400:08:25	992330	< ACK 01		Command: ACK			
	DPDT	DP-R31	+00:08:26	000182	> W:100 LINK BW SET L=1 06		Reply to Read Request.			
	DPDT	DP-RS1	+00:08:26	000262						
	DPLT	DP-RSI	+00:08:26	000332	> WINI LANE COUNT SET LEI BI		00204: LANE_ALIGN_STATUS_UPDATED			
	DEPT	DP-RSL	+00:08:26	1000412		0	Bit Name	Value	Descri	ipts
	DFLT	DP-RSI	400:08:26	190011	S WINZ TRAINING PATTERN SET: Del 21	-	0 INTERIANE SLICH DONE	N(0)		
	DPLT	DP-R31	+00:08:26	107114	< ACK		1 POST LT ADJ REQ IN PROGRESS	N(0)		
	DEDI	DP-RSI	+00:08:26	197110	> WITOS TRAINING_LANED_SET D=4 00 00 00 00		2	0	Reserv	red
	DPLT	DP-R31	+00:08:26	197915	< AUA		3	0	Reserv	red
	DPLT	DP-R31	+00:08:26	201412	> R:202 LANEO_1_STATOS: L=2		1	0	Reserv	red
	DPDT	DP-RSL	+00:08:26	2018/9			5 6 DOWNSTREAM_PORT_STATUS_CHANGED 7 LINK_STATUS_UPDATED 00205: SINK_STATUS Bit Name	N (0)	Repert	rea
	DPLT	DP-R31	+00:08:26	202147	> R:202 LANEO_1_STATOS: L=2			N(0)		
	DPLT	DP-R31	+00:08:26	202414	< DEFER					
	DEPL	DP-R31	+00:08:26	202019	S R:202 LANEO_1_STRIDS: 1=2					
	DPLT	DP-R31	+00:08:26	203140	< DEFER			Value	Descri	pti
	DPLT	DP-R31	+00:08:26	203614	> R:202 LANEO_1_STATOS: L=2		0 SECTIVE PORT 0 STATUS	7(1)		
	DPLT	DP-R31	+00:08:26	203881	< DEFER		1 RECEIVE PORT 1 STATUS	Y(1)		
	DPLT	DP-R31	+00:08:26	204348	> R:202 LANEO_1_STATOS: 1=2		2 STREAM REGENERATION STATUS	N(0)		
	DPLT	DP-R31	+00:08:26	204615	< DEFER		3 4 5		Reserv	red
	DFLT	DP-R31	+00:08:26	205080	> R:202 LANEO_1_STATUS: L=2				Reserv	red
	DPLT	DP-H31	+00:08:26	205347	< DEFER				Reserv	Det
	DPLT	DP-831	+00:08:26	205820	> R:202 LANEO_1_STATUS: L=2		7	0	Resert	red
	DPLT	DP-R31	+00:08:26	206087	< ACR 01 00		100001100 00 0311	1		
	DPLT	DP-R31	+00:08:26	206229	> W:102 TRAINING_PATTERN_SET: L=1 07			× .		
	DFLT	DP-RS1	+00:08:26	206309	< ACA					
	DFLT	DF-R31	+00:08:26	206388	> W:103 TRAINING_LANE0_SET L=4 00 00 00 00					
	DFLT	DF-R31	+00:08:26	200491	< ALA					
	DFLT	DP-831	+00:08:26	210601	> R:202 LANEU 1_STATUS: L=3					
	DFLT	DF-RS1	+00:08:26	210673	< ACK 01 00 00					
_	DEPL	DF-831	+00:08:26	210/91	> R:204 LANE_ALION_STATUS_UPDATED L=2					
	DPDT	DP-831	+00:08:26	210863	< ACK 00 03	4				
	DFLT	DF-831	+00:08:26	210974	> R:206 ADJUST_REQUEST_LANE0_1 L=2	1	<u>e</u>			
	DFLT	DP-R31	+00:08:26	211046	< ACK 44 44	10	T1: < ACK 00 03			

DP 1.4 Source Link Layer Compliance - Test Selection

일 Di	P 1.4a Source CT Core R1.0	-		×
Inst	trument: Al M41d [10.30.196.30] - Connect Cards			
IIIO	CDF Entry Test Selection Test Options / Prev	iew		
Sele	ct All 🗹 🕷 Count Options	EXEC	UTE TE	STS
	AIIY Pd after HPD			^
	4.2.1.1: Source DUT Retry on No-Renly During AUX Read after HPD Plug Event	1	1	
-	4.2.1.2. Source Betry on Invalid Renly During AUX Read after HPD Plug Event	1	1	
,	4 2 1.3: Source Device HPD Event Pulse Length Test	1	1	
>	4.2.1.4: Source Device IRO, HPD Pulse Length Test	1	1	
>	4.2.1.5: Source Device Inactive HPD / Inactive AUX Test	1	1	
~	EDID and DPCD Rd.			
,	4.2.2.1: DPCD Receiver Capability and EDID Read upon HPD Plug Event	1	1	
>	4.2.2.2: DPCD Extended Receiver Capability and EDID Read upon HPD Plug Event	1	1	
>	4.2.2.3: EDID Read	1	1	
>	4.2.2.4: EDID Read Failure #1: I2C-Over-AUX NACK	1	1	
>	4.2.2.5: EDID Read Failure #2: I2C-Over-AUX DEFER	1	1	
>	4.2.2.6: EDID Corruption Detection	1	1	
>	4.2.2.7: Branch Device Detection upon HPD Plug Event	1	1	
>	4.2.2.8: EDID Read on IRQ HPD Event after Branch Device Detection	1	1	
>	4.2.2.9: E-DDC Four Block EDID Read	1	1	
>	4.2.2.10: Link Status/Adjust Request AUX read interval during Link Training	1	1	
~	Link Training			
>	4.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds	1	1	
>	4.3.1.2: Successful Link Training Upon HPD Plug Event	1	1	
>	4.3.1.3: Successful Link Training (Higher Differential Voltage Swing during Clock Recovery)	1	1	
>	4.3.1.4: Successful Link Training to a Lower Link Rate #1: Iterate at Maximum Voltage Swing	1	1	
>	4.3.1.5: Successful Link Training to a Lower Link Rate #2: Iterate at Minimum Voltage Swing	1	1	~
			01.000	
			GLUSE	

DP 1.4 Source Link Layer Compliance Test

Dest Extends Municipures Date Texted 1 Text Name / Details Text Name / Details Operations Operations Operations Operations Operations Text Name / Details Operations	Rass Pass Pass Pass Pass Pass Pass Pass
teedst Name: 0.27.2011 513.45 Mondacture: Date Tested: Mach.72.2013 233 PM Mode Name: Test Name / Details Test Name / Details Test Name / Details 0 01: [1] Link Maintenance test for lane count = 4 and lane rate = 8.10 0 01: [2] After Sym look error on lane 1, Link Maintenance test for lane cou 0 03: [3] After Sym look error on lane 1, Link Maintenance test for lane cou 0 04: [4] After Sym look error on lane 2, Link Maintenance test for lane cou 0 04: [4] After Sym look error on lane 3, Link Maintenance test for lane cou 0 04: [5] After Sym look error on lane 3, Link Maintenance test for lane cou 0 04: [5] After Sym look error on lane 3, Link Maintenance test for lane cou 0 04: [5] After Sym look error on lane 4, Link Maintenance test for lane cou 0 04: [6] After Sym look error on lane 4, Link Maintenance test for lane cou 0 04: [6] After Sym look error on lane 4, Link Maintenance test for lane cou 0 04: [6] After Sym look error on lane 4, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 4, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look error on lane 5, Link Maintenance test for lane cou 0 05: [5] After Sym look e	Status Pass Pass Pass Pass Pass Pass Pass Pa
Dute Testek Much 27, 2019 2393M Veral Status	Status Pass Pass Pass Pass Pass Pass Pass
Verail Status: Fort Tests 1 Test Name / Details TestStatus • Test Name / Details C • Of Iter Oil	Status Pass Pass Pass Pass Pass Pass Pass
 Test Name / Details Test Name / Details I 4.3.2.1; Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol I ter G1: I 111 Link Maintenance test for lane count = 4 and lane rate = 8.10 O 21: [1] Link Maintenance test for lane count = 4 and lane rate = 8.10 O 31: [1] Link Maintenance test for lane cout O 31: [1] Link Maintenance test for lane cout O 31: [1] After Sym lock error on lane 3, Link Maintenance test for lane cou O 41: [4] After Sym lock error on lane 4, Link Maintenance test for lane cou Atter loss of Symbol Lock on lane 4. Link re-training starts after Rpulse. Source DUT reads BNCD address 0200-0205h. Source DUT reads BNCD address 0200-0205h. Source DUT reads Ink Status yithin 100ms. Source DUT sets Thi on all active lanes. CR Lock succeeded on all active lanes. CR Lock succeeded on all active lanes. 	Status Pass Pass Pass Pass Pass Pass Pass
 Test Name / Details Test Name / Details I 4.3.2.1: Successful Link Re-training After IRQ HDD Pulse Due to Loss of Symbol I to construct the second secon	Status Pass Pass Pass Pass Pass Pass Pass Pa
 4.3.2.1: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol I ter D1: I the distribution of t	Pass Pass Pass Pass Pass Pass Pass
 First State of the second secon	Pass Pass Pass Pass Pass Pass
 Ol: [1] Link Maintenance test for lane count = 4 and lane rate = 8.10 O2: [2] After Sym lock error on lane 1, Link Maintenance test for lane cou O3: [3] After Sym lock error on lane 2, Link Maintenance test for lane cou O4: [4] After Sym lock error on lane 3, Link Maintenance test for lane cou O5: [5] After Sym lock error on lane 4, Link Maintenance test for lane cou After loss of Symbol Lock on lane 4. Link re-training starts after TRQ palse. Source DUT easi Link status within 100as. Source DUT start link training Source DUT start link training Source DUT start Ink training lane. Chack succesded on all active lanes. OK succesdor on all active lanes. 	Pass Pass Pass Pass Pass Pass
 Q2: [2] After Sym lock error on lane 1, Link Maintenance test for lane cou Q3: [3] After Sym lock error on lane 2, Link Maintenance test for lane cou Q4: [4] After Sym lock error on lane 3, Link Maintenance test for lane cou Q5: [5] After Sym lock error on lane 4, Link Maintenance test for lane cou After loss of Symbol Lock on lane 4. Link re-training starts after IRG palse. Source DDT reads DPC address 2000-2020h. Source DDT read link statis within 100ms. Source DDT reads DPC address 2000-2020h. Source DDT sets Tink training. Source DDT sets Thick training. Source DDT sets Thick trainse. OK associated on all active lanes. 	Pass Pass Pass Pass
 ▶ ⊕ 03; [3] After Sym lock error on lane 2, Link Maintenance test for lane cou ▶ ⊕ 04; [4] After Sym lock error on lane 3, Link Maintenance test for lane cou ● 05; [5] After Sym lock error on lane 4, Link Maintenance test for lane cou ● After Loss of Symbol lock on lane 4. ■ Link re-training starts after IRD palse. ■ Source DUT reads DKCD address 0200-025h. ■ Source DUT start link training ■ Source DUT start link the and lane comt before TP1 is set. ■ Source DUT sets TP1 on all active lanes. ■ OK Loss succeeded on all active lanes. 	Pass Pass Pass
 Ø d: [4] After Sym lock error on lane 3, Link Maintenance test for lane cou Ø 05: [5] After Sym lock error on lane 4, Link Maintenance test for lane cou After loss of Symbol Lock on lane 4. Link re-training starts after IRQ pulse. Source DUT reads DEC address 2000-0205h. Source DUT reads DEC address 2000-0205h. Source DUT reads Dink status within 100ms. Source DUT sets link brand lane comt before TP1 is set. Source DUT sets TP1 on all active lanes. Ch Lock succeeded on all active lanes. 	Pass Pass
 	Pass
After loss of Symbol Lock on lane 4. Link re-training starts after IRQ pulse. Source DUT reads DRCD address 2020-0205h. Source DUT read link status within 100ms. Source DUT start link training. Source DUT start link training. Source DUT sets link bw and lane count before TP1 is set. Source DUT sets STP1 on all active lanes. CR Lock succeeded on all active lanes.	
 Link re-training starts after IEQ pulse. Source DUT read DEC address 2000-2020h. Source DUT start link status within 10Bss. Source DUT start link training. 	
 Source DUT reads DECD address 0200-0205h. Source DUT reads Ink status within 100ms. Source DUT start link training Source DUT start link by and lane count before TP1 is set. Source DUT sets link by and lane. CR Lock succeeded on all active lanes. 	
 Source DUT read link status within 100ms. Source DUT start link training. Source DUT sets link bw and lane count before TP1 is set. Source DUT sets TP1 on all active lanes. C R Lock succeeded on all active lanes. 	
 Source DUT start link training Source DUT sets link bw and lane count before TP1 is set. Source DUT sets TP1 on all active lanes. CR Lock succeeded on all active lanes. 	
Source DUT sets link bw and lane count before TP1 is set. Source DUT sets TP1 on all active lanes. CR Lock succeeded on all active lanes.	
 Source DUT sets TP1 on all active lanes. CR Lock succeeded on all active lanes. 	
• CR Lock succeeded on all active lanes.	
 Training pattern 2 or 3 or 4 detected after Training pattern 1. 	
For HBR3 source Training pattern 4 detected.	
• Equalization succeeded on all active lanes.	
 Symbol lock succeeded on all active lanes. 	
 All Lanes are Aligned and skewed. 	
 Link compliance training test completed successfully. 	
Link training completed in 19.76 ms, which exceeds the 10ms guideline.	
4.3.2.2: Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock F	Pass
3.3.2.3: Successful Link Re-training Arter IRQ HPD Pulse Due to Loss of Inter-1	Pass
4.3.2.4: Handling of ING HPD Pulse with No Error Status Bits Set.	Pass
24.3.2.5: Lane Count Reduction and Increase.	Pass
nis Onen ACA Data 4.2.2.1. Successful Link Partmining After IPO HDD Duke Due to Loss of Sumbal Losk	
op open ACA base	
strument: [559808 [10.30.196.39]	ontinue Test Execu

DP 1.4 LINK LAYER SINK COMPLIANCE

Sink Link Layer Compliance Approved!

The 980 DP sink (display) link layer compliance tests are ideal for pre-testing your DisplayPort 1.4 display product prior to submission to an Authorized Test Center for approval. Pre-testing provides added assurance that your product will pass at the ATC when submitted. The compliance tests (below right) enable you to view the captured data and detailed test results which help pinpoint the cause of compliance test failures. The link layer compliance test suite now includes tests for forward error correction (FEC). You can link to the aux channel traces in the Aux Channel Analyzer (ACA) to view the root cause of failures (below).



Test Setup for Sink Test

DP Aux Channel Traces – From LLC Test

O	ien Clo	ose Export	Options F	iter Find					b
01	My_DP_AC	CA_Capture] Eve	nts: 356 (1331)						
0	DPHP	DP-710	+00:30:45.91	707 HPD Falling Edge	•	Start Time: +00:30:50.871183			
1	DPHP	DP-710	+00:30:50.86	851 MPD Rising Edge	0	Type: Native			
2	DFHP	DF-710	+00:30:50.86	851 MPD Falling Edge		Direction: Reply			
3	DPHP	DP-710	+00:30:50.86	852 RPD Rising Edge		Commence: Aux			
4	DNAT	DF-710	+00:30:50.86	068 > R:200 SINK COUNT L=6		apry to head hequest.			
5	DNAT	DP-710	+00:30:50.86	141 < ACK 41 04 00 00 80 00		2200: DP1.3 DPCD REV			
6	DNAT	DP-710	+00:30:50.87	824 > R:E TRAINING_AUX_RD_INTERVAL L=1		Bit Name	Value	Description	
7	DNAT	DP-710	+00:30:50.87	897 < ACK 81		***** *********************************			-
8	DNAT	DP-710	+00:30:50.87	966 > R:0 DPCD_REV L=1		3-0 Minor Revision	4		
9	DNAT	DF-710	+00:30:50.87	039 < ACK 14		7-4 Major Revision	1		
10	DNAT	DP-710	+00:30:50.87	110 > R:2200 DP1.3 DPCD_REV L=16		2201 - MAY LINK BATE			
11	DNAT	DP-T10	+00:30:50.87	183 < ACK 14 1E C4 81 01 00 01 80 00 20 04 08		Bit Name	Value	Description	
12	DNAT	DF-710	+00:30:50.87	393 > R:90 FEC CAPABILITY L=1					-
13	DNAT	DP-710	+00:30:50.87	466 < ACK BF		7-0 MAX_LINK_RATE	1Eh	8.1 Gbps/lane	
14	DNAT	DF-710	+00:30:50.87	544 > R:60 DSC SUPPORT L=15					
15	DNAT	DP-T10	+00:30:50.87	617 < ACK 01 21 03 7F FB 07 01 00 00 1F 0E EE	. · · · ·	2202: MAX_LAME_COUNT	Walne	Description	
16	DNAT	DF-710	+00:30:50.87	906 > R:D eDP_CONFIGURATION_CAP L=1					
17	DNAT	DF-710	+00:30:50.87	979 < ACK 00		4-0 MAX_LANE_COUNT	4	4 lanes	
18	DNAT	DP-T10	+00:30:50.87	047 > R:701 EDP_GENERAL_CAPABILITY_1 L=1		5 POST_LT_ADJ_REQ_SUP	N(0)		
19	DNAT	DP-710	+00:30:50.87	120 < ACK 87		6 TPS3_SUPPORTED	Y(1)		
20	DNAT	DP-710	+00:30:50.87	188 > R:702 EDP BACKLIGHT ADJ CAPS L=1		/ ENERNCED_FRAME_CAP	I(I)		
21	DNAT	DP-710	+00:30:50.87	261 < ACK 22		2203: MAX DOWNSPREAD			
22	DNAT	DP-710	+00:30:50.87	331 > R:725 EDF FWHGEN BIT COUNT MIN L=2		Bit Name	Value	Description	
23	DNAT	DP-710	+00:30:50.87	403 < ACK 02 0C					-
24	DNAT	DP-710	+00:30:50.87	482 > R:2E RX_ALPM_CAPABILITIES L=1		0 MAX_DOWNSPREAD	1	Up to 0.5%	
25	DNAT	DF-T10	+00:30:50.87	554 < ACK 03		1 STREAM REGEN_STATUS_CAP	N(0)	Reserved	
26	DNAT	DP-710	+00:30:50.87	624 > W:116 RX_ALPM_CONFIGURATION L=1 01		3	ő	Reserved	
27	DNAT	DF-710	+00:30:50.87	704 < ACK		4	0	Reserved	
28	DHDCP	DP-710	+00:30:50.87	436 > R:69493 RxStatus L=1		5	0	Reserved	
29	DHDCP	DF-710	+00:30:50.87	509 < ACK 00		6 NO_AUX_HANDSBAKE_LINK_TRAININ	5 N(0)		
30	DFLT	DF-710	+00:30:50.93	325 > R:100 LINK BN SET L=2		/ TPS4_SUPPORTED	I(1)		
31	DPLT	DP-710	+00:30:50.93	398 < ACK 1E 04		2204 : NORP			
32	DNAT	DF-710	+00:30:51.03	734 > R:200 SINK COUNT 1=6		Bit Name	Value	Description	
33	DNAT	DP-710	+00:30:51.03	807 < ACK 41 04 00 00 00 00					>

DP 1.4 Link Layer Compliance - Test Selection

1	DP 1.4a Sink CT Core R1.0	-		×
Ins	strument: AL_M41d [10.30.196.30] - Connect Cards			
	CDF Entry Test Selection Test Options / Prev	iew		
Sele	ect All 🛷 🛪 Count Options	EXEC	JTE TES	STS
	AUX Ch. Proto.			^
>	5.2.1.1: Read One Byte from Valid DPCD Address	1	1	
>	5.2.1.2: DPCD Receiver Capability Read (Read 12 Bytes from Valid DPCD Address)	1	1	
>	5.2.1.3: Write One Byte to Valid DPCD Address	1	1	
>	5.2.1.4: Write Nine Bytes to Valid DPCD Addresses	1	1	
>	5.2.1.5: Write EDID Offset (One Byte I2C-Over-AUX Write)	1	1	
>	5.2.1.6: Read One EDID Byte (One Byte I2C-Over-AUX Read)	1	1	
>	5.2.1.7: EDID Read	1	1	
>	5.2.1.8: Illegal AUX Request Syntax	1	1	_
>	5.2.1.9: Glitch Rejection	1	1	
>	5.2.1.10: Interleaved EDID and DPCD Receiver Capability Read	1	1	
>	5.2.1.11: Downstream Stop on MOT Reset	1	1	
>	5.2.1.12: Downstream Stop on Timeout	1	1	
	Sink DPCD Field Impl.			
>	5.2.2.1: Sink Organizationally Unique Identifier (OUI)	1	1	
>	5.2.2.2: Sink Count	1	1	
>	5.2.2.3: Sink Status	1	1	
>	5.2.2.4: Sink Error Count	1	1	
>	5.2.2.5: DPCD Address Range	1	1	
>	5.2.2.6: Number of Receiver Ports	1	1	
>	5.2.2.7: Main Link Channel Coding	1	1	
>	5.2.2.8: ESI Field Mapping	1	1	~
			_	
			CLOSE	

DP 1.4 Link Layer Compliance - Test Results

Compliance Test Results Viewer					
DP 1.4 Sink (1.4 Core R1.0) Compliance Test Results					
Results Name: 03_27_2018_15_56_17_sink Manufacturer:		HTML Report			
Date Tested: March 27, 2018 3:56 PM Model Name:					
Overall Status: CTS 1.4 Core R1.0 - Pass Port Tested: 1					
Test Results					
Test Name / Details	0	Status			
▲ [5,3,1,1: Successful Link Training at All Supported Lane Counts and Link Speeds	~	Pass			
A G Iter 01:		Pass			
\rightarrow \bigcirc 01: Link Training test for lane count = 1 and lane rate = 1.62		Pass			
$\triangleright \bigcirc 02$: Link Training test for lane count = 2 and lane rate = 1.62		Pass			
$\triangleright \ominus 03$: Link Training test for lane count = 4 and lane rate = 1.62		Pass			
$\triangleright \ominus$ 04: Link Training test for lane count = 1 and lane rate = 2.70		Pass			
$\triangleright \ominus$ 05: Link Training test for lane count = 2 and lane rate = 2.70		Pass			
$\triangleright \odot 06$: Link Training test for lane count = 4 and lane rate = 2.70		Pass			
$\triangleright \ominus$ 07: Link Training test for lane count = 1 and lane rate = 5.40		Pass			
$\triangleright \ominus 08$: Link Training test for lane count = 2 and lane rate = 5.40		Pass			
$\triangleright \ominus 09$: Link Training test for lane count = 4 and lane rate = 5.40		Pass			
$\triangleright \ominus 10$: Link Training test for lane count = 1 and lane rate = 8.10		Pass			
$\flat \ominus 11$: Link Training test for lane count = 2 and lane rate = 8.10		Pass			
$b \in 12$: Link Training test for lane count = 4 and lane rate = 8.10		Pass			
5.3.1.2: Successful Link Training with Request of Higher Differential Voltage		Pass			
5.3.1.3: Successful Link Training to a Lower Link Rate Due to Clock Recovery L Solution and Solution and Solution Solution and Solution and Solution Solution and Solution		Pass			
2 5.3.1.4: SUCCESSFUL LINK TRAINING With Request of a change to Fre-Emphasis and Other Ale		Pass			
A there us:		Pass			
 UI: Link Training test for lane Count - 4 and lane rate - 0.10 BED is asserted 		Pass			
Becfrence Source receives AIX ACK at 1 attempts					
Reference Source receives AUX ACK from either write request					
AUX Read 0x2201 (MAX LINK RATE) = 0x1e					
• CR lock succeeded on lane 0					
I iterations to achieve CR lock at VOLTAGE SWING SET = 0 on lane 0					
• CR lock succeeded on lane 1					
Die Open ACA Data 5.3.1.1: Successful Link Training at All Supported Lane Counts and Link Speeds					
Instrument: \$\$\$808.110.30.196.391	•	Continue Test Execution			
australiuelini (sosoon fizanemaanos)		M Class			

HDCP 2.2 SOURCE, SINK & REPEATER COMPLIANCE

HDCP 2.2 Compliance

The 980 HDCP 2.2 compliance tests are ideal for pretesting your DisplayPort source, sink or repeater product prior to submission to an Authorized Test Center for approval. Pre-testing provides assurance that your product will pass at the ATC when submitted. The compliance tests enable you to view the auxiliary channel analyzer traces logged (not shown) during the test to help diagnose the cause of compliance test failures.







Test Setup for Sink Test

HDCP 2.2 Sink Tests - Test Selection

ß	DP HDCP 2.3 TX CT 1.1							-		\times
In	strument: Al_M41d	10.30.196.30] 🗢	Connect	Cards						
	CDF Entr	у		Test Selection	ı	Т	est Options / Prev	view		
Se	lect All 🧹 🗙							EXEC	UTE TE	STS
~	TX with Receive	er								^
>	1A-01: Regula	r Procedure:	With prev	viously connect	ed Receiver (With stored Kn	ו)		1	
>	1A-02: Regula	r Procedure:	With new	ly connected R	eceiver (With	out stored Km)			1	
>	1A-03: Regula	r Procedure:	Receiver	disconnect afte	er AKE_Init				1	
>	1A-04: Regula	r Procedure:	Receiver	disconnect afte	er Km				1	
>	1A-05: Regula	r Procedure:	Receiver	disconnect afte	er locality che	eck			1	
>	1A-06: Regula	r Procedure:	Receiver	disconnect afte	er Ks				1	
>	1A-07: Regula	r Procedure:	Receiver	sends REAUTH	_REQ after Ks	S			1	
>	1A-08: Irregul	ar Procedure:	: Verify Re	eceiver Certifica	ate				1	
>	1A-09: Irregul	ar Procedure:	: SRM						1	
~	1A-10: Irregul	ar Procedure:	: Invalid H	ľ					1	
	 Iter 01: Invalid 	I H'							1	
	 Iter 02: H' Tim 	eout with previ	ously paire	d Recv Id					1	
	 Iter 03: H' Tim 	eout with previ	ously unpa	ired Recv Id					1	
>	1A-11: Irregul	ar Procedure:	: Pairing F	ailure					1	
>	1A-12: Irregul	ar Procedure:	: Locality	Failure					1	
	1A-13: Regula	r Procedure -	Encrypti	on Disable Boo	tstrapping				1	
	Iter 01: Encryp	otion Disable Bo	ootstrappin	g not supported: /	Automatic PAS	S(SKIP)			1	
v	TX with Repeat	er								
>	1B-01: Regula	r Procedure:	With Rep	eater					1	
>	1B-02: Irregul	ar Procedure:	: Timeout	of Receiver ID	list				~	
>	1B-03: Irregul	ar Procedure:	: Verify V						1	~
									_	
									CLOSE	

HDCP 2.2 Source Tests - Test Selection

일 D	P HDCP 2.3 TX CT 1.1	-		×
Ins	strument: AL_M41d [10.30.196.30] - Connect Cards			
	CDF Entry Test Selection Test Options / P	review		
Sele	ect All 🧭 🕱	EXE		
~	TX with Receiver			^
>	1A-01: Regular Procedure: With previously connected Receiver (With stored Km)		1	
>	1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)		1	
>	1A-03: Regular Procedure: Receiver disconnect after AKE_Init		1	
>	1A-04: Regular Procedure: Receiver disconnect after Km		1	
>	1A-05: Regular Procedure: Receiver disconnect after locality check		1	
>	1A-06: Regular Procedure: Receiver disconnect after Ks		1	
>	1A-07: Regular Procedure: Receiver sends REAUTH_REQ after Ks		1	
>	1A-08: Irregular Procedure: Verify Receiver Certificate		1	
>	1A-09: Irregular Procedure: SRM		1	
~	1A-10: Irregular Procedure: Invalid H'		1	
	Iter 01: Invalid H'		1	
	 Iter 02: H' Timeout with previously paired Recv Id 		1	
	 Iter 03: H' Timeout with previously unpaired Recv Id 		1	
>	1A-11: Irregular Procedure: Pairing Failure		1	
>	1A-12: Irregular Procedure: Locality Failure		1	
~	1A-13: Regular Procedure - Encryption Disable Bootstrapping		1	
	 Iter 01: Encryption Disable Bootstrapping not supported: Automatic PASS(SKIP) 		1	
~	TX with Repeater			
>	1B-01: Regular Procedure: With Repeater		1	
>	1B-02: Irregular Procedure: Timeout of Receiver ID list		×	
>	1B-03: Irregular Procedure: Verify V		×	~
			CLOS	E

HDCP 2.2 Source Tests - Test Results

Compliance Test Results Viewer		
DP HDCP 2.2 TX (1.0) Compli:	ance Test Results	
Results Name: Acme_DP_HCDP_Src_Results_3 Manufacturer: A	cme	HTML Report
Date Tested: January 20, 2017 6:39 PM Model Name: XX	YZ	
Overall Status: CTS 1.0 - Incomplete Port Tested: 1		
Test Devolte		
Termsus		Status
First Name / Decails	9	status
A E IA-UI: Regular Procedure: With previously connected Receiv	er (With stored Km)	Pass
12 12 00: Demiles Decembers, With scale second Deciders (*	the set of the set of the set	Pass
FIA-02: Regular Procedure: With newly connected Receiver (w 13-03: Regular Procedure: Receiver disconnect after AVE In	1thout stored Km)	Pass
The Distance of the Distance o		Page
9 TX AUTH: MSG: HPD DIS ta: 7561890365.44 pa		1433
TX: UNAUTH : : ENTER		
9 TX UNAUTHINSO RDINPD DIS ta:0.00 pa		
9 TX UNAUTH: MSG RD: INVALID VER ts: 32966939792173888.00 us		
9 EX UNAUTH::ENTER Rep:no DevCnt:0 Dep:0		
9 RX UNAUTH:NO VIDEO Present		
9 TX UNAUTH: MSG RD: VALID VER ts: 7563890841.60 us		
9 TX UNAUTH:MSG RD:HPD EN ts:7565890877.44 us		
• TX UNAUTH: ARE INIT ts: 7565891379.20 us		
• TX UNAUTH:MSG RD:AKE Init ts:7565891379.20 us		
• RX UNAUTH:RCVD:ARE Init ts:7565891317.76 us		
RX UNAUTH:**Test Cond.** hpd		
• TX UNAUTH:MSG RD:HPD DIS ts:7565893928.96 us		
• TX UNAUTH:MSG RCVD:AKE Send Cert ts:0.00 us		
Warn: AKE SEND CERT not rovd within 100ms of AKE INIT		
• TX UNAUTH: RxCaps 2 0 2		
• Failed to verify the signature on Receiver certificate		
• TX UNAUTH:MSG RD:VALID_VER ts:7567892224.00 us		
• TX UNAUTH: MSG RD: HPD_EN ts: 7569892382.72 us		
 RX UNAUTH:RCVD:ARE_Init ts:7569892833.28 us 		
• RX UNAUTH:**Test Cond.** ake_init		
• RX UNAUTH:Encryption Disabled		
• RX ARE::enter		
b 1A-04: Regular Procedure: Receiver disconnect after Km		Pass
IA-05: Regular Procedure: Receiver disconnect after locali	ty check	Pass
IA-06: Regular Procedure: Receiver disconnect after Ks		Pass
IA-07: Regular Procedure: Receiver sends REAUTH REQ after	Ks	Pass
D 1A-08: Irregular Procedure: Verify Receiver Certificate		Pass
IA-09: Irregular Procedure: SRM		Incomplete
IA-10: Irregular Procedure: Invalid H'		Pass
IA-11: Irregular Procedure: Pairing Failure		Pass
IA-12: Irregular Procedure: Locality Failure		Pass
Image: Procedure - Encryption Disable Bootstrappin	g	Incomplete

HDCP 2.2 Sink Tests – Test Results

Compliance Test Results Viewer	- • ×
DP HDCP 2.2 Receiver (1.0) Compliance Test Results	
Results Name: Acme XYZ HDCP 22 DP Sink 1 Manufacturer: Acme	HTML Report
Date Tested: January 24, 2017 11:51 AM Model Name: XYZ	
Overall Status: CTS 1.0 - Incomplete Port Tested: 1	
Test Results	
Test Name / Details	Status
▶ 2C-01: Begular Procedure - With transmitter	Pass
2C-02: Irregular Procedure - New Authentication after AKE Init	Pass
2C-03: Irregular Procedure - New Authentication during Locality Chec	k Pass
2C-04: Irregular Procedure - New Authentication after SKE Send Eks	Pass
A Diter 01:	Pass
TX: HPD:: ENTER	
• TX HPD:**Test Cond.** ake init	=
• TX UNAUTH :: ENTER	
• RX MSG RD:ENC DIS ts:92078933053.44 us	
Encryption Disabled	
• TX UNAUTH:AKE INIT ts:92080432230.40 us	
 TX UNAUTH:MSG RD:AKE Init ts:92080432230.40 us 	
 RX AUTH:MSG RCVD:AKE Init ts:92080432179.20 us 	
HDCP2RX:UNAUTH Rep:no DevCnt:31 Dep:4	
• MSG RCVD:AKE Init ts:92080432179.20 us	
RX MSGR:WROTE to DPCD:AKE Send Cert:534 ts:92080432414.72	
• TX UNAUTH:MSG RCVD:ARE Send Cert ts:92080491888.64 us	
• TX UNAUTH:Rrx ff,ca,f8,b,25,72,82,f2	
• TX UNAUTH:RxCaps 2 0 2	
RX:AKE:MSG SND:AKE_Send_Cert ts:92080505088.00 us	
MSG RCVD:AKE_Stored_km ts:92080506019.84 us	
 TX AKE:Snd Stored KM ts:92080506081.28 us 	
RX MSGR:WROTE to DPCD:AKE Send H prime:33 ts:92080506091.52	
 TX AKE:MSG:AKE_Stored_km ts:92080506081.28 us 	
• TX AKE:MSG RCVD:AKE_Send_H_prime ts:92080510832.64 us	
 TX LC:Snd LC Init ts:92080511948.80 us 	
 TX LC:MSG:LC_Init ts:92080511948.80 us 	
 MSG RCVD:LC Init ts:92080511887.36 us 	
• RX MSGR:WROTE to DPCD:LC_Send_L_prime:33 ts:92080512256.00	
RX:SKE: MSG SND:AKE Send H prime ts:92080511887.36 us	

EMBEDDED DISPLAYPORT (EDP) 1.4B TESTING

Embedded DisplayPort eDP - ALPM

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer supports testing of both eDP source and display subsystems. A standard DP connection from the 980 DP 1.4 eDP-capable module to a test fixture is required to enable connection to the eDP subsystem. For display panel TCON testing, once the connection is made, you can use the Advanced Link Power Management (ALPM) feature to test the display's ALPM function (right) and run any other video tests using the DP 1.4 module's Video Generation function. For eDP source subsystem testing, you can monitor the link training and ALPM state and run captures for analysis, etc. The test setups are shown below.



Test Setup for eDP TCON Display Subsystem



Test Setup for testing eDP source Subsystem

eDP Fast Link Training

The 980 DP 1.4 USB-C/eDP Video Generator / Analyzer supports fast link training acting either as an eDP source subsystem or an eDP display subsystem. The module emulates the necessary Fast Link training DPCD registers When testing a display you can select the Lane Count, Link rate (including "intermediate "eDP lane rates), Voltage Swing, Pre-Emphasis and Training Test Pattern. You can monitor the Aux Channel transactions with the 980 Aux Channel Analyzer utility. (eDP Fast Link Training Source test not shown.)

eDP Tx Backlight Control

The 980 DP 1.4 USB-C/eDP module supports testing of the eDP backlight control function on eDP TCON display subsystems. Backlight control is supported through the Aux Channel and the backlight control lead. The connection is made through the module's eDP header pins on the faceplate. You can select between High and Low backlight enable, set the PWM duty cycle, pre-scaling and PWM generator divider.

Advanced Link Power Management (ALPM)



Link Training Control and Configuration



Auxiliary Channel Analyzer – Fast Link Train



eDP Tx Backlight Control



SPECIFICATIONS

DisplayPort 1.4 / USB-C/ eDP Module

Vereien	Dianley Dort 1 4a					
Version Ctandard Formata						
Stanuaru Formats	VESA, UTA					
	Tx (1) USB C with DD Alt Mode: Dx (1) USB C with DD Alt Mode					
ODD Header	Pine to access a DD Tx backlight controls					
Aux Chan Adjunct Board	Ty (1) DD Full-cize Dy (1) DD Full-cize					
Protocol	DisplayPort					
11010001	1 62 2 7 5 4 8 1 Gb/s Link rates					
Video Data Rates	1.2.4 Lanes					
Color Depths	8, 10, 12, 16 bits					
Video Encoding	RGB, YCbCr					
Video Sampling Modes	4:4:4, 4:2:2, 4:2:0					
HDCP	Versions 2.2 & (1.3 on 1 & 2 lanes only)					
Audio	8 Channel LPCM programmable sine wave					
Capture memory	8 GBytes					
Options						
options	Fisher er hethe					
DisplayPort Tx / Rx	 DP Tx for display testing; selectable between DP Standard and USB-C DP Rx port, two options; selectable between DP Standard and USB-C: Basic Analyzer Capture/Store Protocol Analyzer (requires Basic analyzer option) 					
DP Passive Aux Channel Analyzer	Monitor DisplayPort Aux Channel transactions in real time passively between a source or sink. Includes custom cable and Aux Adjunct board.					
DP Capture Analysis of DSC Streams	Capture and analyze incoming Display Stream Compression (DSC) streams. There are no limits on the number of DSC slices for analysis.					
DP Video Generation of DSC/FEC	Select from a variety of DSC/FEC test patterns. Select colorimetry and configure slices.					
Streams	There are no limits on the number of DSC slices supported.					
DP HDCP 2.2 Compliance Test	Run HDCP 2.2 compliance test on DisplayPort sources, sinks and repeaters (3 separate options) – Now Approved by DCP.					
DP 1.4 Source Link Layer Compliance (Package #3)	Run DisplayPort 1.4 source Link Layer compliance test. (Sections: 4.3.1, 4.3.2, 4.3.3, 4.4.4, 4.5.1 [FEC])					
DP 1.4 Sink Link Layer Compliance (Package #4)	Run DisplayPort 1.4 sink Link Layer compliance test (displays). (Sections: 5.2.1, 5.3.1, 5.3.2, 5.4.1/2 5.4.3, 5.4.4, 5.5.1 [FEC].)					
DP 1.4 Sink EDID Compliance.	Run DisplayPort 1.4 sink EDID/DisplayID compliance test (displays).					
NEW! DP 1.4 Source EDID Comp.	Run DisplayPort 1.4 source EDID/DisplayID compliance test.					
DP 1.4 Source DSC/FEC Compliance	Run DisplayPort 1.4 source DSC/FEC compliance test Sections. 4.6.1/4.5.1.1. Requires 64-bit 980 system.					
DP 1.4 Sink DSC/FEC Compliance	Run DisplayPort 1.4 Sink DSC/FEC compliance test. Sections 5.6.1, 5.6.2/5.5.1.1					
Embedded DisplayPort (eDP) 1.4b	Test eDP source and display devices using fast link training, Advanced Link Power Management (ALPM) and backlight control testing of displays.					
980 Test Platforms						
Embedded Display	980B: 15" diagonal; Resolution: 1024(H); x 768 (V) resolution; 24 bit RGB color. 980R: 7" diagonal: Resolution: 800 (H) x 480 (V); 24 bit RGB color.					
Power	90-264 VAC, 47-63Hz					
Weight	23.76 LBS; 10.78 Kg					
Size	980B: Height: 15.25 in. (38.7cm) Width: 14.57in. (36.5cm) Depth: 6.29in. (15.9cm) 980R: Height: 6.29 in. (15.9cm); Width: 15.25in. (38.7cm); Depth: 14.57in. (36.5cm					
Command Line Control	Ethernet (RJ-45) for external GUI and telnet					
Environmental	Operating Temp: 32 to 104 (F); 0 to 40 (C)					



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