

# quantumdata Product Family

## 980 48G Video Analyzer/Generator Product Overview

March – 2021



**TELEDYNE LECROY**  
Everywhereyoulook™



**980 Test System  
showing 48G Protocol Analyzer/  
Video Generator module  
for HDMI 2.1 Testing**

# quantumdata Product Family...Our Mission:

*Help silicon and product developers bring their next-generation video solutions to market—faster, without interoperability problems and at reduced cost*



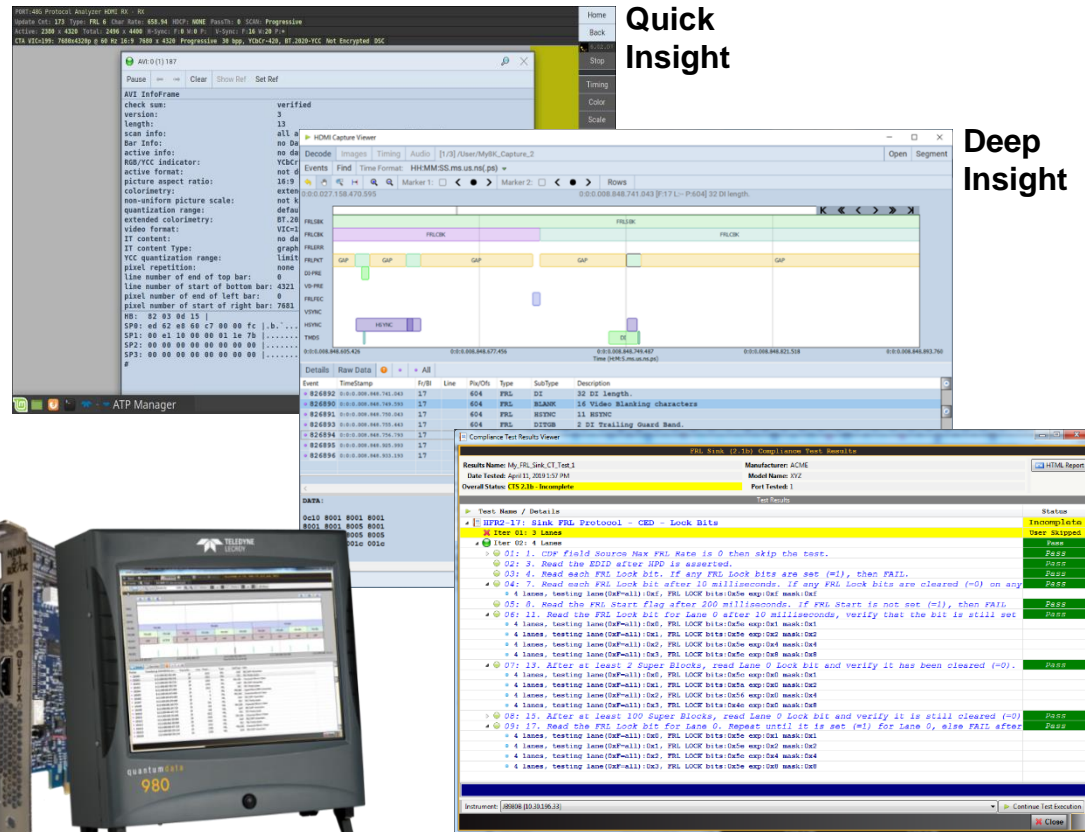
Our solutions quicken Time-to-Insight



# What is Time-to-Insight?

◆ **Time-to-Insight saves time and money.** It involves the following:

- ◆ **Quick Insight:** Provides at-a-glance information—insight—into the basic functioning of an HDMI video device or system.
- ◆ **Deep Insight:** Provides full visibility—insight—into the low level protocol to verify the proper functioning of an HDMI device to improve interoperability.
- ◆ **Compliance Tests:** Provides required test suites for HDMI, Logo program.



Compliance

## ◆ Quick Insight Solutions Include:

- ◆ Real Time analysis views of incoming videos streams.
- ◆ Essential status information on dashboards, and status panels.
- ◆ Device emulation of sources and sinks (displays).

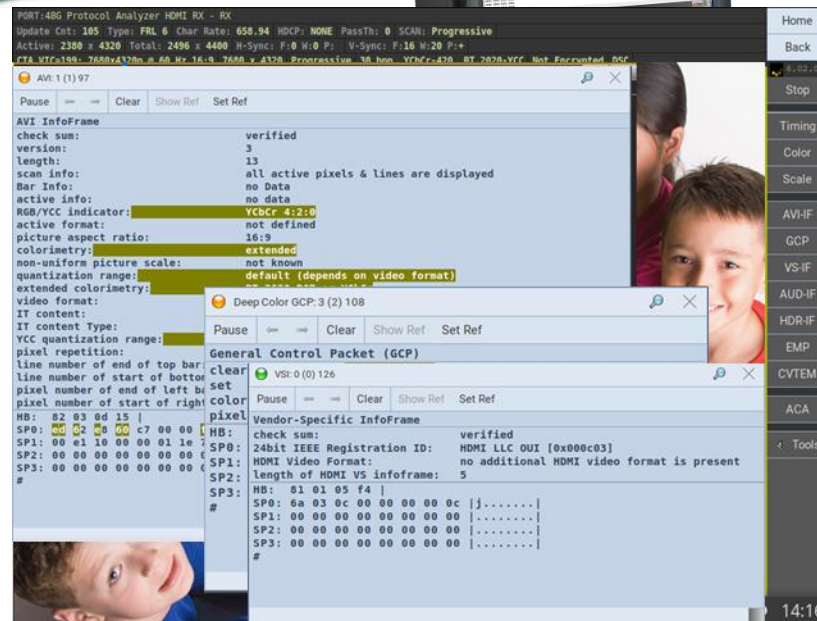
## ◆ A Few Examples:

- ◆ HDMI Real Time view w/ status bar at top. Shows incoming video and metadata from a source device. ➔
- ◆ DisplayPort link training control & status with connected display. ➔
- ◆ HDMI EDID and SCDC data view of connected sink device. ➔

HDMI 2.1 source development board



890B w/ 48G HDMI Protocol Analyzer / Video Generator module



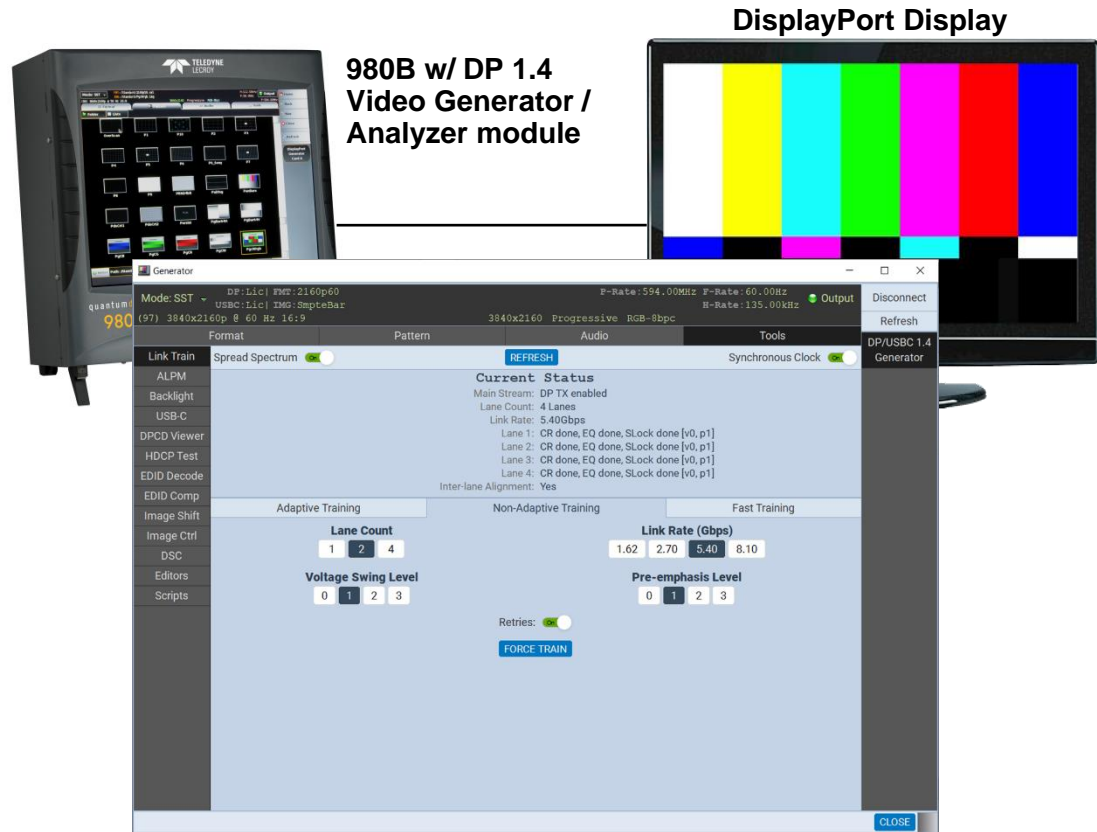


## ◆ Quick Insight Solutions Include:

- ◆ Real Time analysis views of incoming videos streams.
- ◆ Essential status information on dashboards, and status panels.
- ◆ Device emulation of sources and sinks (displays).

## ◆ A Few Examples:

- ◆ HDMI Real Time view w/ status bar at top. Shows incoming video and metadata from a source device. ➔
- ◆ DisplayPort link training control & status with connected display. ➔
- ◆ HDMI EDID and SCDC data view of connected sink device. ➔

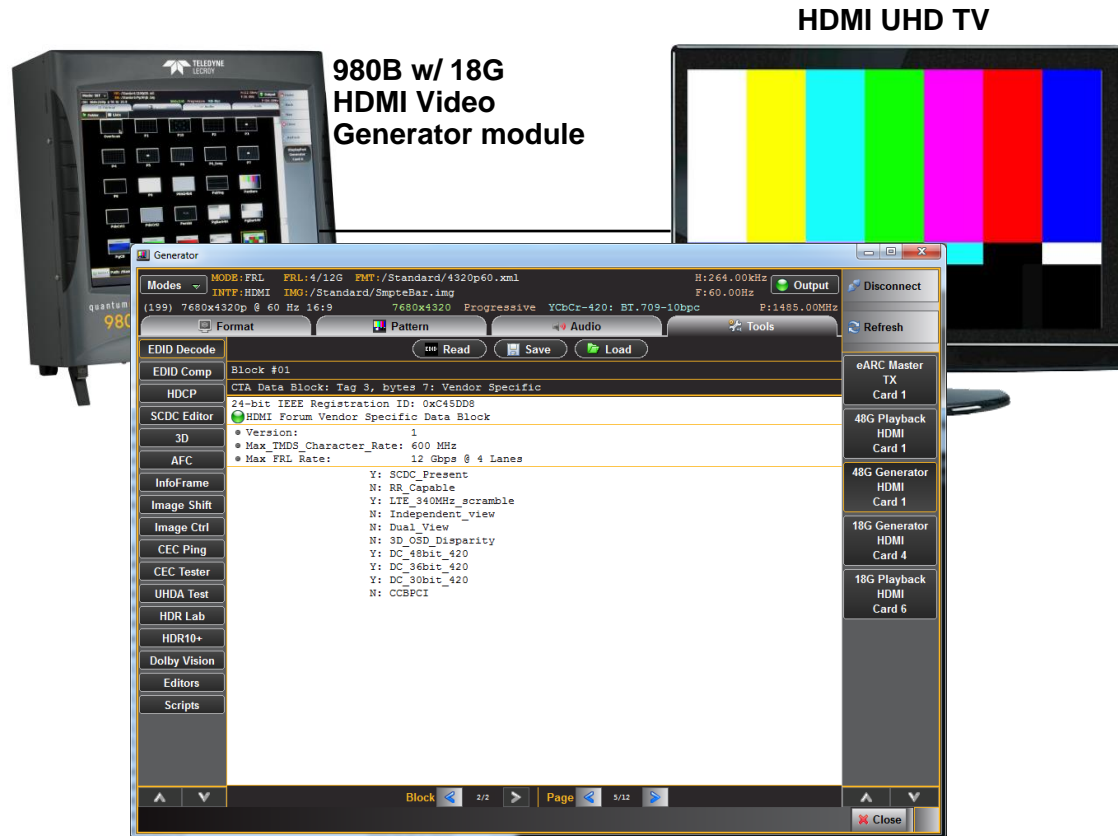


## ◆ Quick Insight Solutions Include:

- ◆ Real Time analysis views of incoming videos streams.
- ◆ Essential status information on dashboards, and status panels.
- ◆ Device emulation of sources and sinks (displays).

## ◆ A Few Examples:

- ◆ HDMI Real Time view w/ status bar at top. Shows incoming video and metadata from a source device. ➔
- ◆ DisplayPort link training control & status with connected display. ➔
- ◆ HDMI EDID and SCDC data view of connected sink device. ➔



## ◆ Deep Insight offers:

- ◆ In depth analysis of the low level protocol operation over the main video transmission link.
- ◆ Analysis of connection sequence protocol transactions over the auxiliary channel.

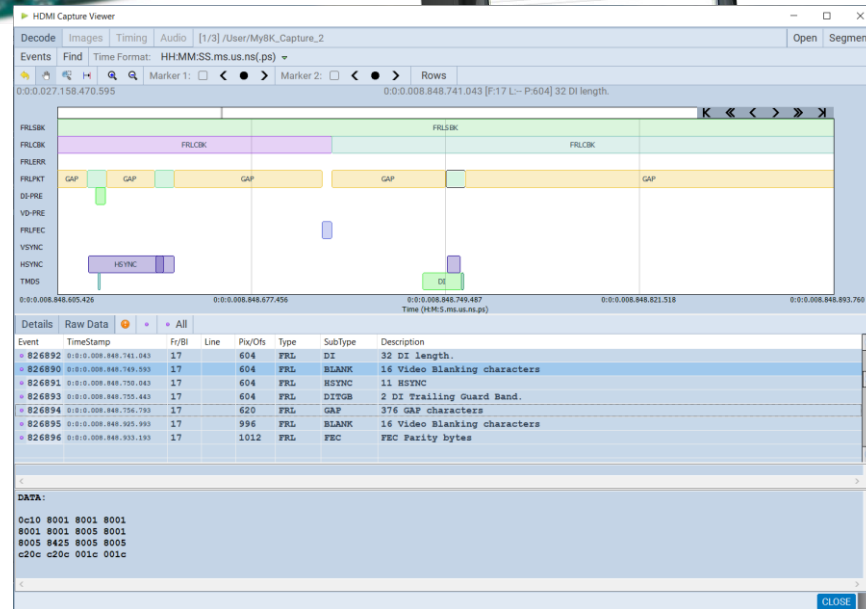
## ◆ A Few Examples:

- ◆ HDMI capture & analysis of HDMI 2.1 Fixed Rate Link (FRL) transmission providing full visibility into the FRL and TMDS protocol stream. →
- ◆ DisplayPort 1.4 capture & analysis of 8.1Gb/s main stream. →
- ◆ Analysis of HDMI 2.1 FRL Link Training transactions. →

HDMI 2.1 source development board



980B w/ 48G HDMI Protocol Analyzer / Video Generator module





# Deep Insight – Example 1

## ◆ Deep Insight offers:

- ◆ In depth analysis of the low level protocol operation over the main video transmission link.
- ◆ Analysis of connection sequence protocol transactions over the auxiliary channel.

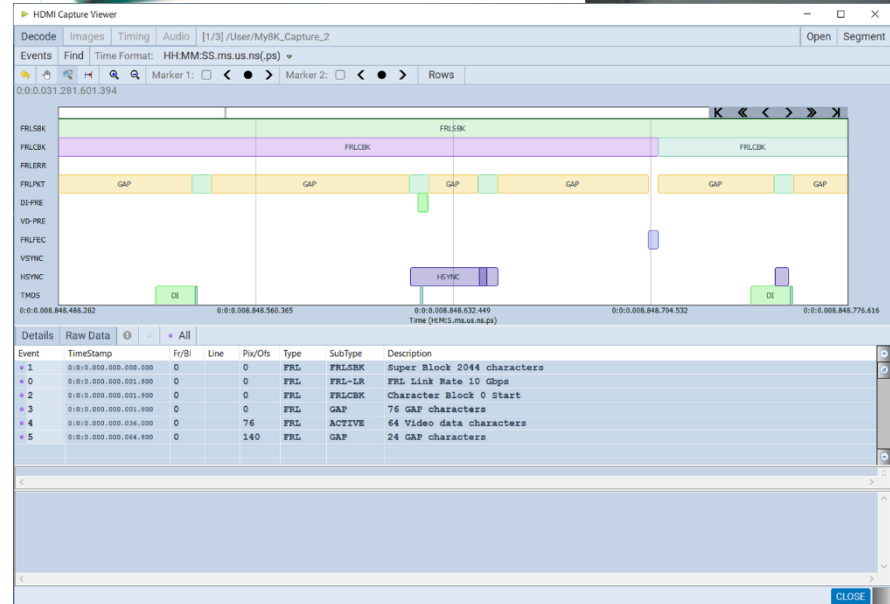
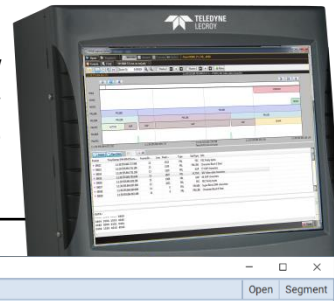
## ◆ A Few Examples:

- ◆ HDMI capture & analysis of HDMI 2.1 Fixed Rate Link (FRL) transmission providing full visibility into the FRL and TMDS protocol stream.

HDMI 2.1 source development board

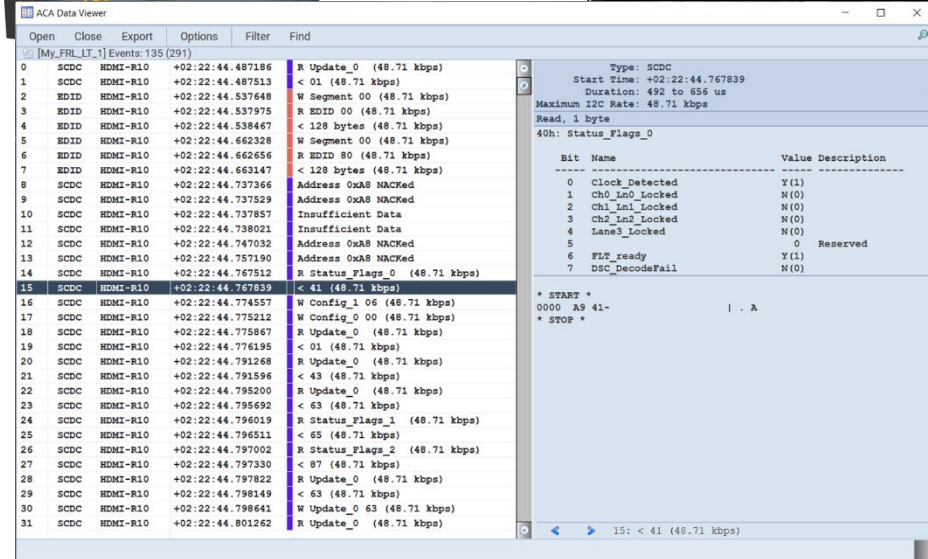


980B w/ 48G HDMI Protocol Analyzer / Video Generator module





- ◆ Analysis of HDMI 2.1 FRL Link Training transactions.



## ◆ Compliance Testing Provides:

- ◆ Required test suites to obtain industry logo.
- ◆ Detailed test results and logs that provide insight into the cause of failures.

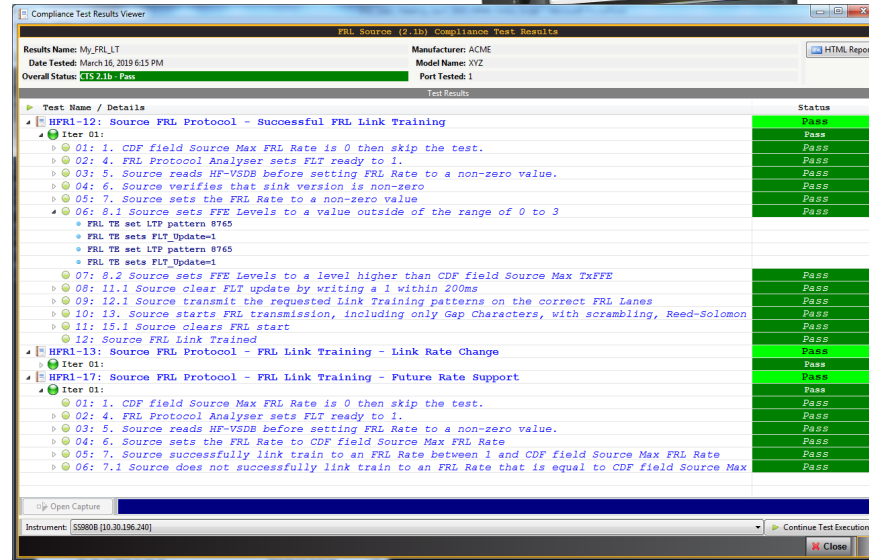
## ◆ A Few Examples:

- ◆ HDMI 2.1 Fixed Rate Link (FRL) source compliance test suite. ➔
- ◆ DisplayPort 1.4 sink compliance for Display Stream Compression (DSC). ➔
- ◆ HDCP 2.2 compliance for HDMI source devices. ➔

HDMI 2.1 source development board



980B w/ 48G HDMI Protocol Analyzer / Video Generator module



# Compliance Testing

## ◆ Compliance Testing Provides:

- ◆ Required test suites to obtain industry logo.
- ◆ Detailed test results and logs that provide insight into the cause of failures.

## ◆ A Few Examples:

- ◆ HDMI 2.1 Fixed Rate Link (FRL) source compliance test suite. ➔
- ◆ DisplayPort 1.4 sink compliance for Display Stream Compression (DSC). ➔
- ◆ HDCP 2.2 compliance for HDMI source devices. ➔



980B w/ 48G module  
Video Generator /  
Analyzer module

DP DSC Display



Compliance Test Results Viewer

DP 1.4a DSC Sink (R1.0) Compliance Test Results

Results Name: DSC\_sink\_test  
Date Tested: May 21, 2019 4:26 PM  
Overall Status: **15 RLO - Pass**  
Manufacturer:  
Model Name:  
Port Tested: 1

Test Results

Test Name / Details	Status
5.6.1.1: DSC capability verification	Pass
Iter 01:	Pass
01: Verify DSC capability.	Pass
DSC and FEC both supported by Sink DUT.	
All DSC capability registers (60h-6fh) are valid and as per specs.	
5.6.1.2: DSC RGB color depth test	Pass
Iter 01:	Pass
5.6.1.4: DSC RGB bits-per-pixel test	Pass
Iter 01:	Pass
01: Initial Link Training at maximum link rate and lane count success	Pass
02: For Timing 1920x1080p830Hz bpc 8 bpp 8.0 CRC check or Visual check verification	Pass
03: For Timing 1920x1080p830Hz bpc 8 bpp 8.125 CRC check or Visual check verification	Pass
04: For Timing 1920x1080p830Hz bpc 8 bpp 8.250 CRC check or Visual check verification	Pass
05: For Timing 1920x1080p830Hz bpc 8 bpp 8.375 CRC check or Visual check verification	Pass
06: For Timing 1920x1080p830Hz bpc 8 bpp 10.0 CRC check or Visual check verification	Pass
07: For Timing 1920x1080p830Hz bpc 8 bpp 10.125 CRC check or Visual check verification	Pass
08: For Timing 1920x1080p830Hz bpc 8 bpp 10.250 CRC check or Visual check verification	Pass
After Sending DSC image 2K1r5q.dpx. Timing 1920x1080p830Hz, Color RGB	
Slice-Width=960, Slice-Height=1080, Bits-per-component=8, Bits-per-pixel=10.250000, Block-Prediction=Enable	
TEST_CRC_R_Cr 0x0E98 matched with expected value.	
TEST_CRC_G_Y 0x886F matched with expected value.	
TEST_CRC_B_Cb 0x4475 matched with expected value.	
DSC_CRC_0 0xc455 matched with expected value.	
DSC_CRC_1 0xdA23 matched with expected value.	
DSC_CRC_2 0x417D matched with expected value.	
09: For Timing 1920x1080p830Hz bpc 8 bpp 10.375 CRC check or Visual check verification	Pass
10: For Timing 1920x1080p830Hz bpc 10 bpp 8.0 CRC check or Visual check verification	Pass
11: For Timing 1920x1080p830Hz bpc 10 bpp 8.125 CRC check or Visual check verification	Pass
12: For Timing 1920x1080p830Hz bpc 10 bpp 8.250 CRC check or Visual check verification	Pass
13: For Timing 1920x1080p830Hz bpc 10 bpp 8.375 CRC check or Visual check verification	Pass

Open ACA Data 5.6.1.1: DSC capability verification

Instrument: 5980B (10.30.196.240)

Continue Test Execution

Close

## ◆ Compliance Testing Provides:

- ◆ Required test suites to obtain industry logo.
- ◆ Detailed test results and logs that provide insight into the cause of failures.

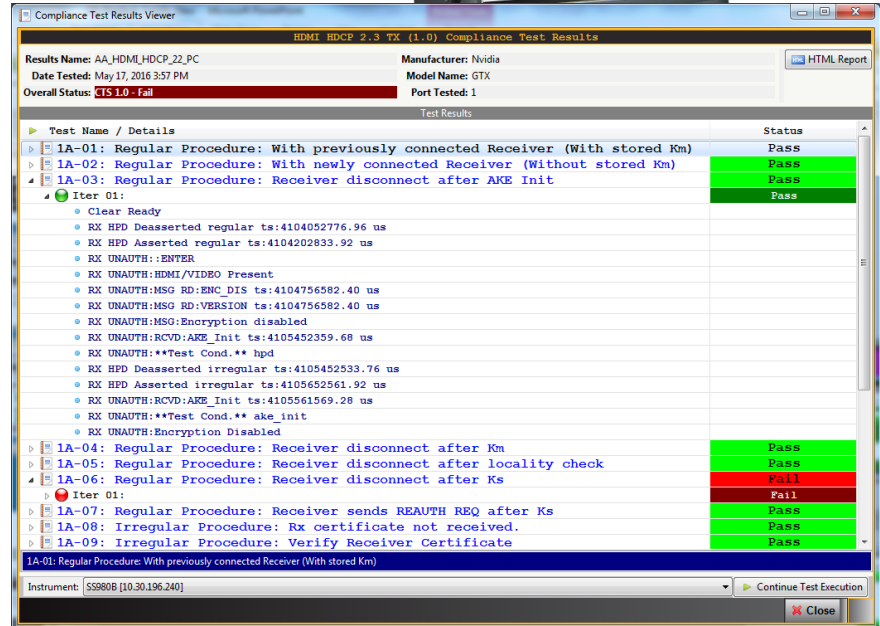
## ◆ A Few Examples:

- ◆ HDMI 2.1 Fixed Rate Link (FRL) source compliance test suite. ➔
- ◆ DisplayPort 1.4 sink compliance for Display Stream Compression (DSC). ➔
- ◆ HDCP 2.2 compliance for HDMI source devices. ➔

HDMI 2.1 source



980B w/ 48G HDMI Protocol Analyzer / Video Generator module



Compliance Test Results Viewer

HDMI HDCP 2.3 TX (1.0) Compliance Test Results

Results Name: AA.HDMI.HDCP\_22\_PC      Manufacturer: Nvidia  
Date Tested: May 17, 2016 3:57 PM      Model Name: GTX  
Overall Status: **CIS 1.0 - Fail**      Port Tested: 1

Test Results

Test Name / Details	Status
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	Pass
1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	Pass
1A-03: Regular Procedure: Receiver disconnect after AKE Init	Pass
Iter 01:	Pass
Clear Ready	
RX HPD Deasserted regular ts:4104052776.96 us	
RX HPD Asserted regular ts:4104202833.92 us	
RX UNAUTH::ENTER	
RX UNAUTH:HDMI/VIDEO Present	
RX UNAUTH:MSG RD:ENC_DIS ts:4104756582.40 us	
RX UNAUTH:MSG RD:VERSION ts:4104756582.40 us	
RX UNAUTH:MSG:Encryption disabled	
RX UNAUTH:RCVD:AKE_Init ts:4105452359.68 us	
RX UNAUTH:**Test Cond.** hpd	
RX HPD Deasserted irregular ts:4105452533.76 us	
RX HPD Asserted irregular ts:4105652561.92 us	
RX UNAUTH:RCVD:AKE_Init ts:4105561569.28 us	
RX UNAUTH:**Test Cond.** ake_init	
RX UNAUTH:Encryption Disabled	
1A-04: Regular Procedure: Receiver disconnect after Km	Pass
1A-05: Regular Procedure: Receiver disconnect after locality check	Pass
1A-06: Regular Procedure: Receiver disconnect after Ks	Fail
Iter 01:	Fail
1A-07: Regular Procedure: Receiver sends REAUTH REQ after Ks	Pass
1A-08: Irregular Procedure: Rx certificate not received.	Pass
1A-09: Irregular Procedure: Verify Receiver Certificate	Pass
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	

Instrument: S980B [10.30.136.240]      Continue Test Execution



# HDMI Compliance Tests – Example 1

## ◆ Compliance Testing Provides:

- ◆ Required test suites to obtain industry logo.
- ◆ Detailed test results and logs that provide insight into the cause of failures.

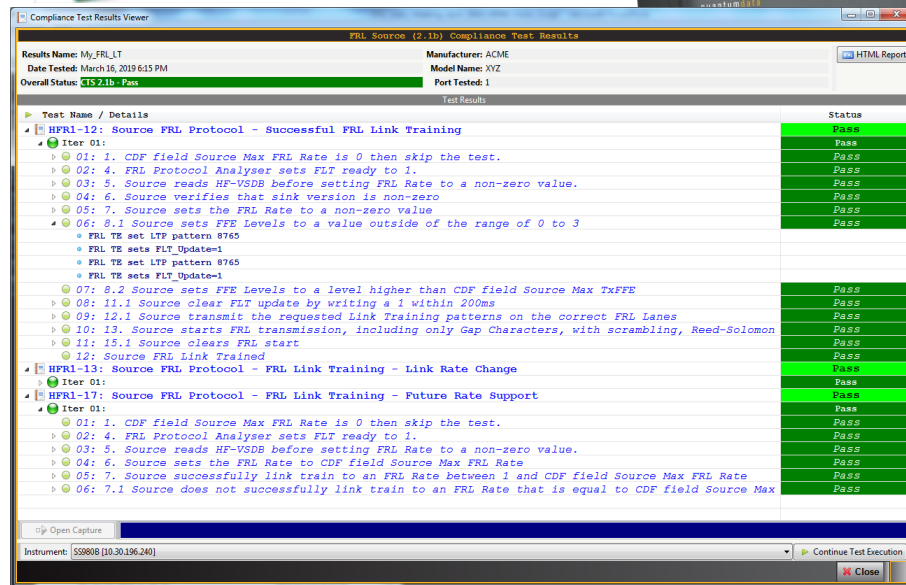
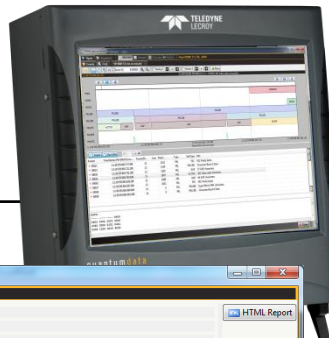
## ◆ A Few Examples:

- ◆ HDMI 2.1 Fixed Rate Link (FRL) source compliance test suite.

HDMI 2.1 source development board



980B w/ 48G HDMI Protocol Analyzer / Video Generator module





# HDMI Compliance Tests – Example 2

## ◆ Compliance Testing Provides:

- ◆ Required test suites to obtain industry logo.
- ◆ Detailed test results and logs that provide insight into the cause of failures.

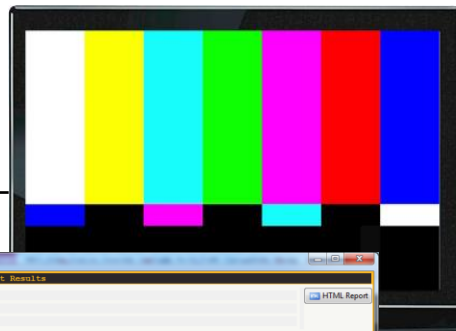
## ◆ A Few Examples:

- ◆ HDMI sink compliance for Forward Error Correction (FEC).



980B w/ 48G HDMI  
Protocol Analyzer /  
Video Generator  
module

HDMI FRL UHD Display



Compliance Test Results Viewer

Results Name: AA\_NVR\_RL\_48\_Full  
Date Tested: December 11, 2018 11:14 AM  
Overall Status: **115.21% Pass**  
Manufacturer: qd  
Model Name: 980  
Port Tested: 1

Test Name / Details	Status
HFPR2-48: Sink FRL Protocol - RS - Basic Operation	Pass
Iter 01: 3 Lanes	Pass
Iter 02: 4 Lanes	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 4. Read the RSCC, verify that RS C Valid flag = 0; otherwise FAIL.	Fail
03: 7. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all active Lanes, else FAIL after 200 milliseconds	Pass
04: 8. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after 200 milliseconds	Pass
05: 10. Read the RSCC, verify that RS C Valid flag = 1 and count =0 or 1; otherwise FAIL.	Pass
06: 11. Corrupt symbols at a rate of about 1e-9, spaced out over 10 seconds, with 1 error/block.	Pass
07: 12. Read the RSCC; if the value is not correct within 1 count then FAIL.	Pass
08: 13. Read the RSCC again after 100 milliseconds; if the count is not 0 or 1 then FAIL.	Pass
09: 14. Corrupt symbols at a rate of about 2e-9, spaced out over 10 seconds, with 2 errors/block in evenly-spaced blocks.	Pass
10: 15. Read the RSCC; if the value is not correct within 1 count then FAIL.	Pass
11: 16. Corrupt one symbol in each of 4 consecutive RS blocks, after generating the RS data	Pass
12: 17. Change the FRL data stream to be random data on all lanes.	Pass
13: 18. After 5 seconds, read each FRL Lock bit and verify that they have all been cleared = 0.	Pass
14: 19. Read the RSCC, verify that RS C Valid flag = 1; otherwise FAIL	Pass
15: 20. If the count in the RSCC is less than 4, then FAIL.	Pass
HFPR2-49: Sink FRL Protocol - RS - Correction Counting During Reads	Fail
Iter 01:	Fail
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 2. Perform Link Training at the minimum FRL Rate with the maximum number of FRL Lanes supported by the sink.	Pass
03: 4. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all active Lanes, else FAIL after 200 milliseconds	Pass
04: 7. Read the RSCC, verify that RS C Valid flag = 1 and count =0 or 1; otherwise FAIL.	Pass
05: 8. Corrupt one symbol in each of a known random number (between 10000 and 30000) of RS blocks over a 1-second period.	Pass
06: 9. 100 milliseconds after the start of the symbol error, read the RSCC and add the value to a cumulative count.	Pass
07: 11.1. If the correction count is outside the range of 12 from the number of generated symbol errors, then FAIL.	Fail
RS errs 19962 instead of between 19998-20000	Fail
HFPR2-50: Sink FRL Protocol - RS - Maximum Symbol Error Count	Pass
HFPR2-51: Sink FRL Protocol - RS - Update Flag with Specific Symbol Error Count	Pass
HFPR2-52: Sink FRL Protocol - RS - Update Flag with Maximum Symbol Error Count	Pass
HFPR2-48: Sink FRL Protocol - RS - Basic Operation	Pass

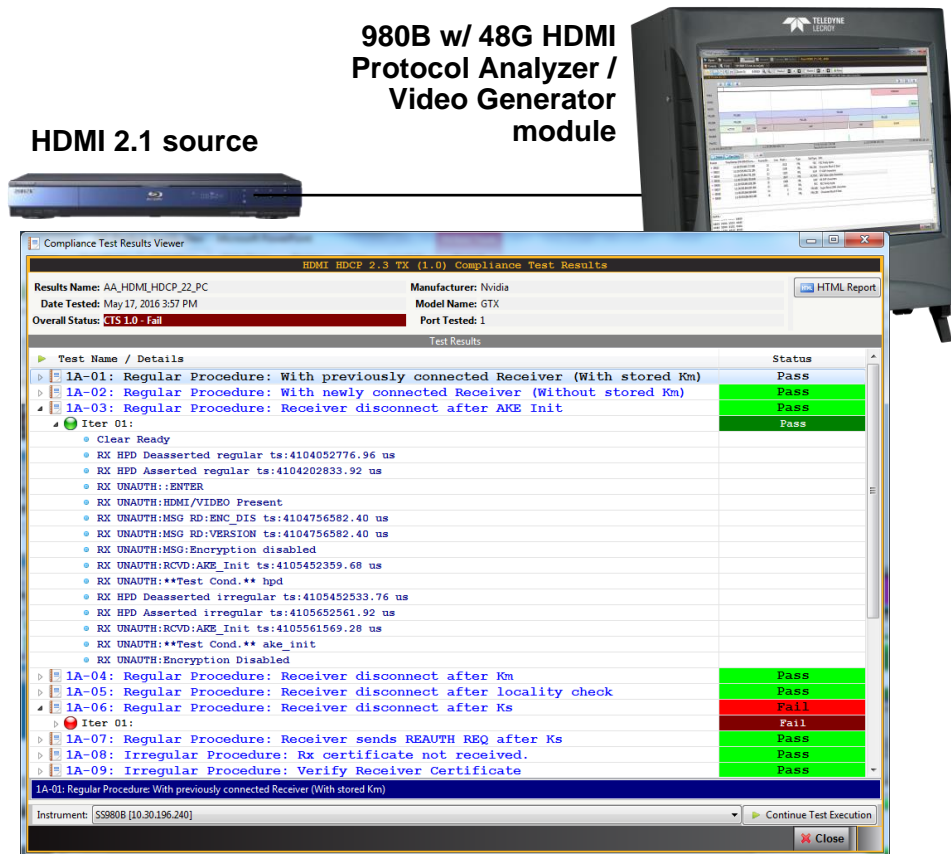
Instrument: PQ808B (10.30.136.17) [Continue Test Execution] [Close]

# HDMI Compliance Tests – Example 3

- ◆ Compliance Testing Provides:
  - ◆ Required test suites to obtain industry logo.
  - ◆ Detailed test results and logs that provide insight into the cause of failures.
- ◆ A Few Examples:
  - ◆ HDCP 2.2 compliance for HDMI source devices.

**980B w/ 48G HDMI Protocol Analyzer / Video Generator module**

**HDMI 2.1 source**



**Compliance Test Results Viewer**

HDMI HDCP 2.2 TX (1.0) Compliance Test Results

Results Name: AA\_HDMI\_HDCP\_22\_PC      Manufacturer: Nvidia  
Date Tested: May 17, 2016 3:57 PM      Model Name: GTX  
Overall Status: **Fail**      Port Tested: 1

Test Results

Test Name / Details	Status
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	Pass
1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	Pass
1A-03: Regular Procedure: Receiver disconnect after AKE Init	Pass
Iter 01:	Pass
Clear Ready	
RX HPD Deasserted regular ts:4104052776.96 us	
RX HPD Asserted regular ts:4104202833.92 us	
RX UNAUTH::ENTER	
RX UNAUTH:HDMI/VIDEO Present	
RX UNAUTH:MSG RD:ENC_DIS ts:4104756582.40 us	
RX UNAUTH:MSG RD:VERSION ts:4104756582.40 us	
RX UNAUTH:MSG:Encryption disabled	
RX UNAUTH:RCVD:AKE_Init ts:4105452359.68 us	
RX UNAUTH:**Test Cond.** hpd	
RX HPD Deasserted irregular ts:4105452533.76 us	
RX HPD Asserted irregular ts:4105652561.92 us	
RX UNAUTH:RCVD:AKE_Init ts:4105561569.28 us	
RX UNAUTH:**Test Cond.** ake_init	
RX UNAUTH:Encryption Disabled	
1A-04: Regular Procedure: Receiver disconnect after Km	Pass
1A-05: Regular Procedure: Receiver disconnect after locality check	Pass
1A-06: Regular Procedure: Receiver disconnect after Ks	Fail
Iter 01:	Fail
1A-07: Regular Procedure: Receiver sends REAUTH REQ after Ks	Pass
1A-08: Irregular Procedure: Rx certificate not received.	Pass
1A-09: Irregular Procedure: Verify Receiver Certificate	Pass
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	

Instrument: S980B [10.30.196.240]      Continue Test Execution

# quantumdata 980 48G module Video Analyzer/Generator Test Setups

November - 2019

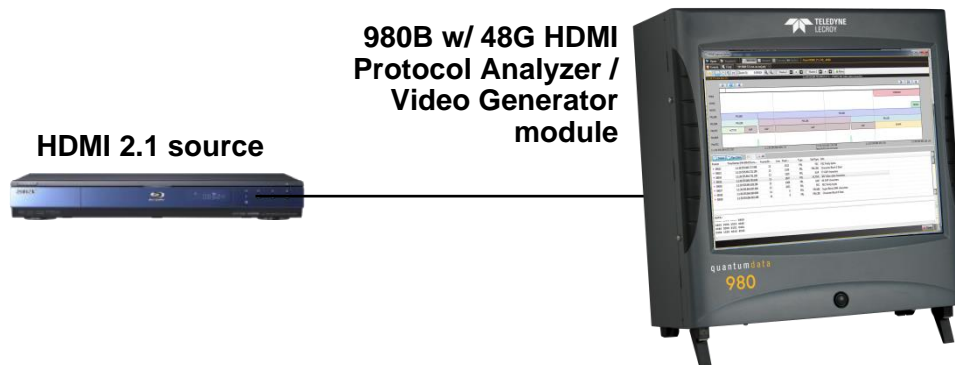


**TELEDYNE LECROY**  
Everywhereyoulook™

# 980 48G module Test Setup – HDMI Source Testing

## ◆ Source testing

- ◆ Use connected HDCP 2.3 compatible display to view 980 48G module ATP Manager Graphical User Interface.
- ◆ Connection either to DisplayPort or HDMI port on back of 980 48G module.
- ◆ Use Keyboard and mouse to control ATP Manager GUI running on the connected display.



# 980 48G module Test Setup – HDMI Sink Testing

## ◆ Sink testing

- ◆ Use connected 980 48G module ATP Manager graphical user interface installed on host PC.
- ◆ Use Keyboard and mouse to control ATP Manager GUI running on the connected display.
- ◆ Connect Host PC to 980 48G module via Ethernet cable, either direct or through corporate LAN.



980B w/ 48G HDMI  
Video Generator /  
Analyzer module

DP DSC Display

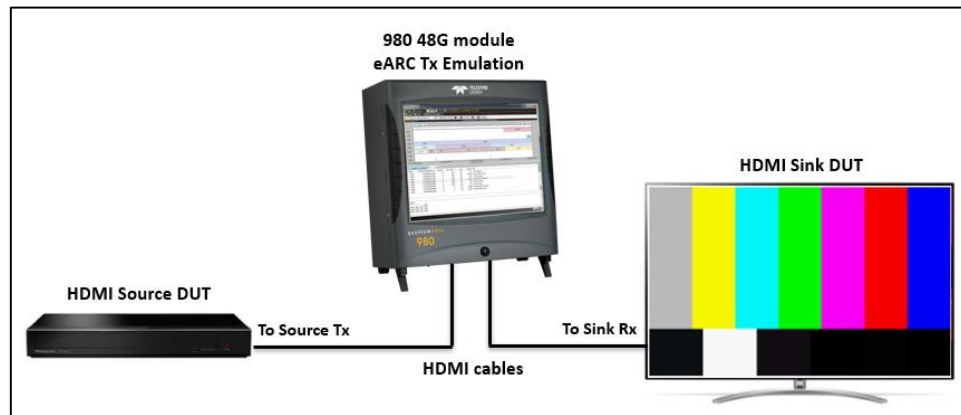
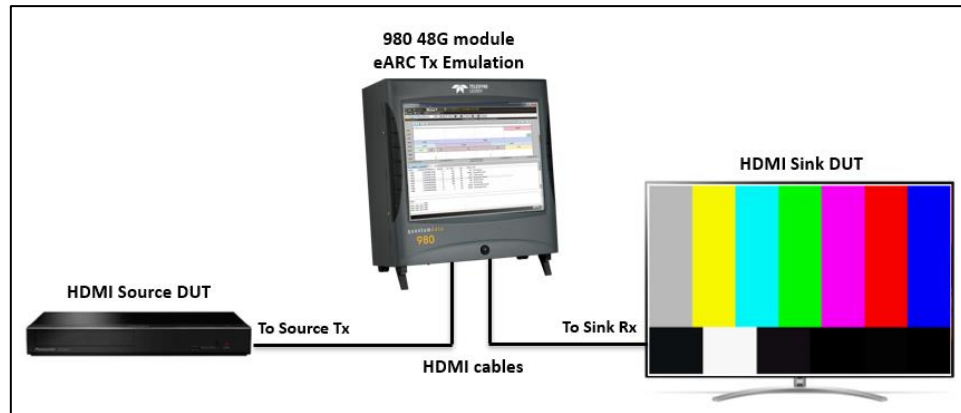




# 980 48G module Test Setup – Passive Monitoring TMDS and FRL

## ◆ Passive monitoring of DDC

- ◆ You can monitor the DDC channel passively in the **TMDS** mode by connecting a source to the 980 48G module Rx port and a sink to the 980 48G module Tx port.
- ◆ You can optionally monitor the DDC channel passively in the **FRL** mode using a custom cable.
- ◆ The DDC passive monitoring enables you to diagnose interoperability problems between a source and a display.
- ◆ The ability to passively monitor the DDC channel in the FRL mode with the custom cable is especially important for FRL link training and HDCP authentication interoperability.



# quantumdata 980 48G Module Video Analyzer/Generator for HDMI Testing Product Details

November - 2019



**TELEDYNE LECROY**  
Everywhereyoulook™

# 980 48G Module Video Analyzer / Generator for HDMI 2.1 Testing

- ◆ Provides both Protocol Analysis for FRL / TMDS source testing and Video Generation for FRL / TMDS sink testing.
- ◆ Supports Real Time view of incoming video and essential video parameters.
- ◆ Protocol Analyzer provides deep visibility into the HDMI 2.1 Fixed Rate Link (FRL), FRL with Display Stream Compression (DSC) and TMDS video, audio, metadata, control data and protocol data.
- ◆ Monitors DDC activity: EDID, HDCP and FRL link training with Aux Channel Analyzer (ACA) utility.
- ◆ Video Generator supports HDMI 2.1 FRL and TMDS outputs up to 1485MHz pixel rate for 8K.
- ◆ Supports HDMI 2.1 FRL and TMDS compliance testing for HDMI sources and sinks up to 8K format resolutions.
- ◆ Supports testing of eARC Tx and Rx devices including full compliance testing for both Common mode and Differential mode.



# Table of Contents – Link to Sections

## ◆ Source Testing

- ◆ Real Time Analysis. [→](#)
- ◆ Deep Capture Analysis. [→](#)
- ◆ DDC (Aux Chan) Monitoring. [→](#)
- ◆ FRL and TMDS Compliance. [→](#)
- ◆ HDCP Compliance. [→](#)
- ◆ eARC Rx Testing. [→](#)
- ◆ DDC (Aux Chan) Monitoring. [→](#)
- ◆ Passive DDC Monitoring. [→](#)

## ◆ Sink Testing

- ◆ Video Generation. [→](#)
- ◆ InfoFrame/Data Island Editing. [→](#)
- ◆ Audio Generation. [→](#)
- ◆ EDID and SCDC. [→](#)
- ◆ FRL and TMDS Compliance. [→](#)
- ◆ HDCP Compliance. [→](#)
- ◆ eARC Tx Testing. [→](#)



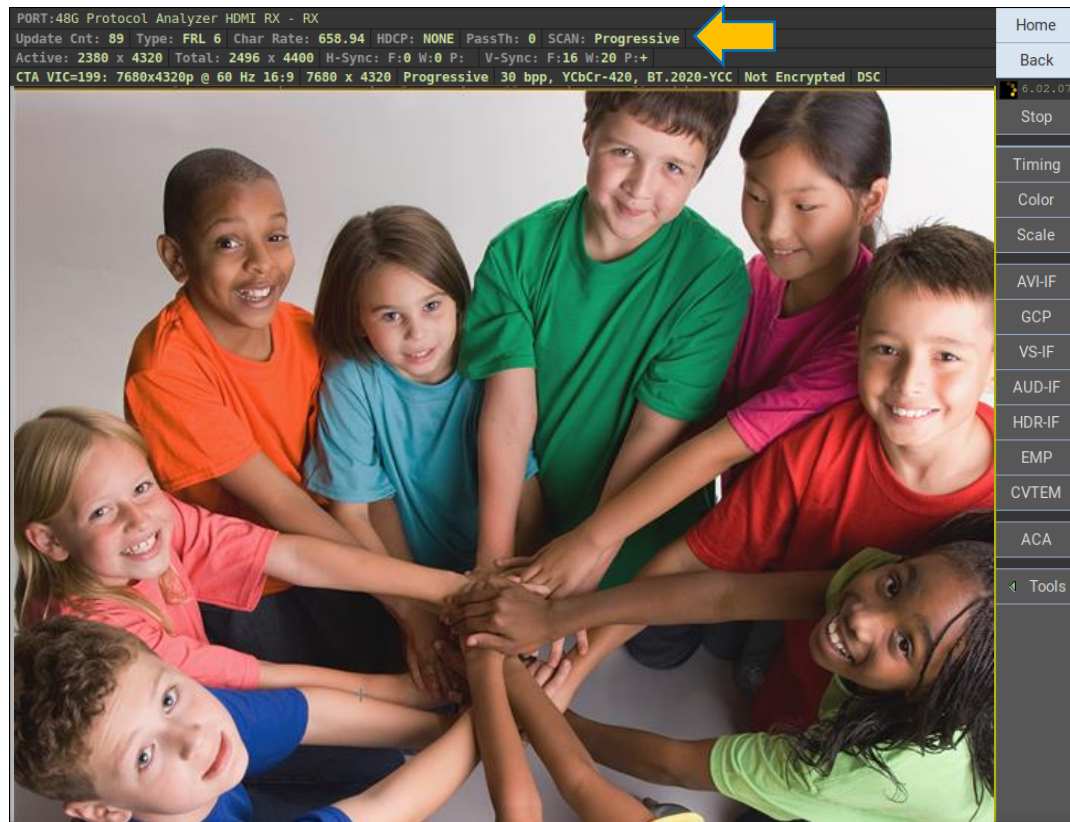
# HDMI 2.1 Source Testing Real Time Analysis



# HDMI Protocol Analyzer – Real Time Analysis

## ◆ HDMI FRL & TMDS Real Time Analysis:

- ◆ Enables viewing of the incoming video frames.
- ◆ Shows essential video metadata and timing data and FRL link configuration on status bar.



# HDMI Protocol Analyzer – Real Time Analysis

## ◆ HDMI FRL & TMDS Real Time Analysis:

- ◆ Enables viewing of the incoming video frames.
- ◆ Shows essential video metadata and timing data and FRL link configuration on status bar.
- ◆ Shows incoming Display Stream Compression (DSC) frame and indicates if DSC is active.

The screenshot displays the PORT:486 Protocol Analyzer HDMI RX - RX interface. The top status bar shows the following information: Update Cnt: 89, Type: FRL 6, Char Rate: 658.94, HDCP: NONE, PassTh: 0, SCAN: Progress, Active: 2380 x 4320, Total: 2496 x 4400, H-Sync: F:0 W:0 P: V-Sync: F:16 W:20 P:+, CTA VIC=199: 7680x4320p @ 60 Hz 16:9, 7680 x 4320 Progressive 30 bpp, YCbCr-420, BT.2020-YCC Not Encrypted DSC. Two yellow arrows point to the 'DSC' and 'YCbCr-420' text in the status bar. The main window shows a video frame of a group of children. An 'AVI:1 (1) 97' window is open, displaying the following AVI infoframe data:

AVI InfoFrame	
check sum:	verified
version:	3
length:	13
scan info:	all active pixels & lines are displayed
Bar Info:	no data
active info:	no data
RGB/YCC indicator:	YCbCr 4:2:0
active format:	not defined
picture aspect ratio:	16:9
colorimetry:	extended
non-uniform picture scale:	not known
quantization range:	default (depends on video format)
extended colorimetry:	BT.2020 RGB or YCbCr
video format:	VIC=199 (7680x4320p @ 59.94Hz/60Hz)
IT content:	no data
IT content Type:	graphics Not used - IT content bit (IT) bit is set to 0
YCC quantization range:	limited range
pixel repetition:	none
line number of end of top bar:	0
line number of start of bottom bar:	4321
pixel number of end of left bar:	0
pixel number of start of right bar:	7681
HB:	82 03 0d 15
SP0:	cd 02 00 c7 00 00 fc   .b   . . .
SP1:	00 e1 10 00 00 01 1e 7b   . . . . . {
SP2:	00 00 00 00 00 00 00 00   . . . . . }
SP3:	00 00 00 00 00 00 00 00   . . . . . }
#	



# Protocol Analyzer – Real Time Analysis

- ◆ HDMI FRL & TMDS Real Time Analysis:
  - ◆ Enables viewing of the incoming video frames.
  - ◆ Shows essential video metadata and timing data and FRL link configuration on status bar.
  - ◆ Provides a real time view of each metadata packet type and the values and change history for each parameter.

The screenshot displays the PORT:486 Protocol Analyzer HDMI RX - RX interface. The top status bar shows: Update Cnt: 105, Type: FRL 6, Char Rate: 658.94, HDCP: NONE, PassTh: 0, SCAN: Progressive, Active: 2380 x 4320, Total: 2496 x 4400, H-Sync: F:0 W:0 P: V-Sync: F:16 W:20 P:+, CTA VTR=199, 7680x4320 @ 60 Hz 16:9, 7680 x 4320, Progressive, 30 bnn, YCbCr-420, RT, 2020-VCC, Not Encrypted, DSC.

The main window shows the AVI (1) 97 packet details:

- check sum: verified
- version: 3
- length: 13
- scan info: all active pixels & lines are displayed
- Bar Info: no Data
- active info: no data
- RGB/YCC indicator: YCbCr 4:2:0
- active format: not defined
- picture aspect ratio: 16:9
- colorimetry: extended
- non-uniform picture scale: not known
- quantization range: default (depends on video format)
- extended colorimetry: default (depends on video format)
- video format: default (depends on video format)
- IT content: IT content Type: YCC quantization range: pixel repetition: line number of end of top bar: line number of start of bottom pixel number of end of left bar pixel number of start of right bar

The bottom window shows the Vendor-Specific InfoFrame (VS: 0 (0) 126) details:

- check sum: verified
- 24bit IEEE Registration ID: HDMI LLC OUI [0x000c03]
- HDMI Video Format: no additional HDMI video format is present
- length of HDMI VS infoframe: 5
- HB: 81 01 05 f4
- SP0: 6a 03 0c 00 00 00 00 0c | j.....|
- SP1: 00 00 00 00 00 00 00 00 | .....|
- SP2: 00 00 00 00 00 00 00 00 | .....|
- SP3: 00 00 00 00 00 00 00 00 | .....|

# Protocol Analyzer – Real Time Analysis

## ◆ HDMI FRL & TMDS Real Time Analysis:

- ◆ Enables viewing of the incoming video frames.
- ◆ Shows essential video metadata and timing data and FRL link configuration on status bar.
- ◆ Provides a real time view of each metadata packet type and the values and change history for each parameter.
- ◆ Emulate a variety of EDIDs and SCDC capability configurations to test an HDMI source's response.

The screenshot displays the 48G Protocol Analyzer HDMI RX - RX interface. The top status bar shows: Update Cnt: 105, Type: FRL 6, Char Rate: 658.94, HDCP: NONE, PassTh: 0, SCAN: Progressive, Active: 2380 x 4320, Total: 2496 x 4400, H-Sync: F:0 W:0 P:+, V-Sync: F:16 W:20 P:+, CTA VTR=199: 7680x4320n @ 60 Hz 16:9 7680 x 4320 Progressive 30 bps VChCr:420 RT 2020-VCC Not Encrypted DSC, and AVI: 1 (3) 9514. The AVI InfoFrame window is open, showing a left sidebar with tabs: Status, Hot-Plug, 5-Volts, SCDC, HDCP, and Analysis. The 'Status' tab is selected. A 'REFRESH' button is at the top right of the status window. The status data includes: State: :LTS\_P, Lanes: :4, Rate: :10 GHz, MAX FFE: :0, FLT\_NO\_TO: :0, FRL\_MAX: :0, LTP: :5:6:7:8, Valid GAP Chrs received: YES, Valid Super Block structure: YES, Disparity: lock: CDR Errors, Ln\_0 : 0:NO:NO, Ln\_1 : 0:NO:NO, Ln\_2 : 0:NO:NO, Ln\_3 : 0:NO:NO, FEC Corrupted Code Block Count: 0, and FEC Symbol Error Count: 0. A 'CLOSE' button is at the bottom right of the status window. The background shows a video frame of a person's face.

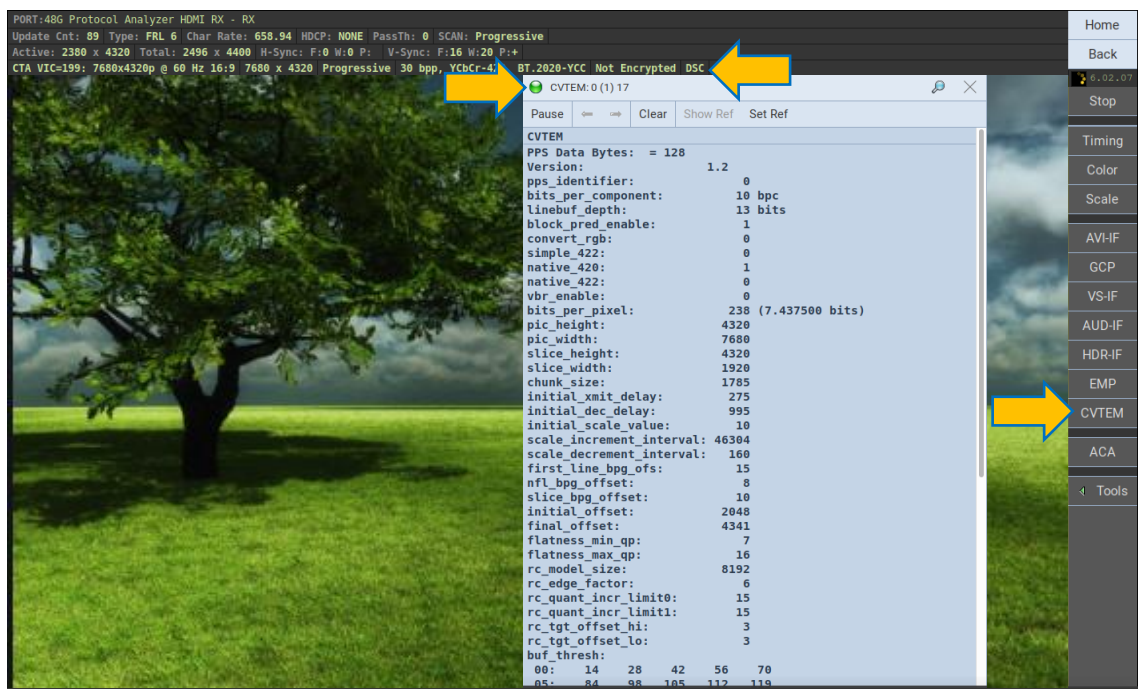
Parameter	Value
State	:LTS_P
Lanes	:4
Rate	:10 GHz
MAX FFE	:0
FLT_NO_TO	:0
FRL_MAX	:0
LTP	:5:6:7:8
Valid GAP Chrs received	YES
Valid Super Block structure	YES
Disparity	lock: CDR Errors
Ln_0	: 0:NO:NO
Ln_1	: 0:NO:NO
Ln_2	: 0:NO:NO
Ln_3	: 0:NO:NO
FEC Corrupted Code Block Count	0
FEC Symbol Error Count	0





# Protocol Analyzer – Real Time Analysis with DSC

- ◆ HDMI FRL & TMDS Real Time Analysis:
  - ◆ Enables viewing of the incoming Display Stream Compression (DSC) video frames.
  - ◆ Indicates that DSC is active on the status bar.





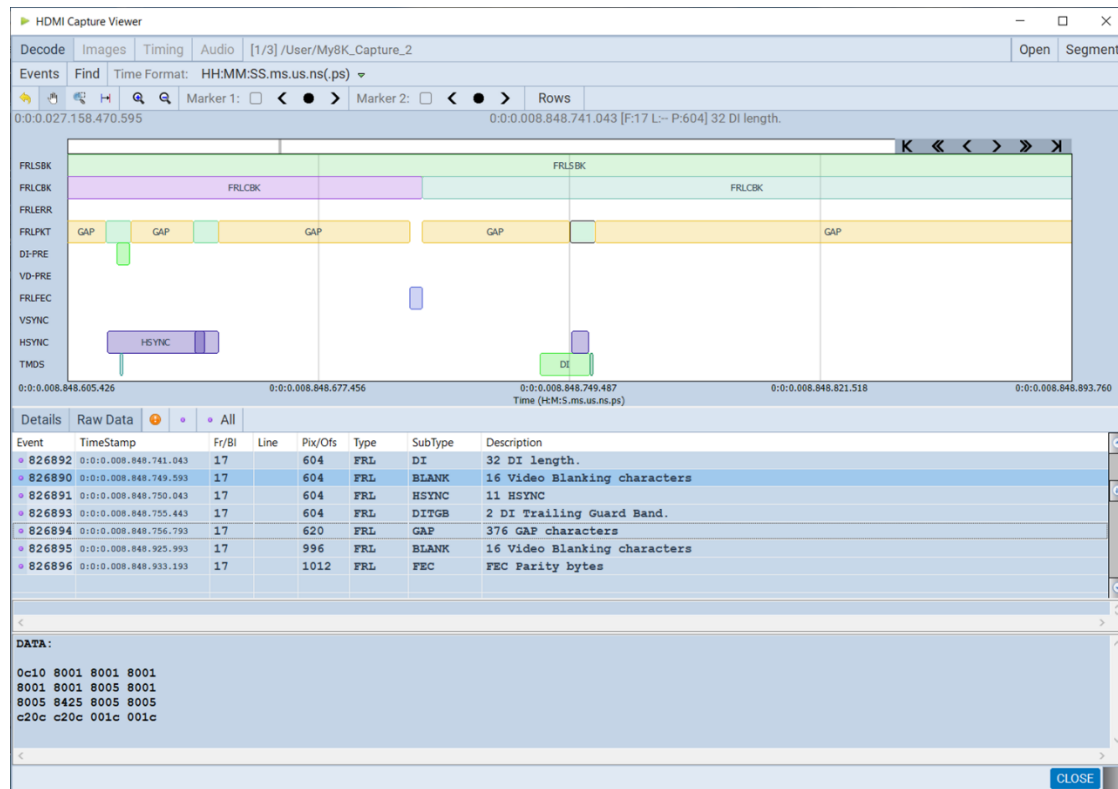
# HDMI 2.1 Source Testing Capture Analysis



# HDMI FRL Protocol Analysis

## ◆ HDMI FRL Capture & Store for Protocol Analysis:

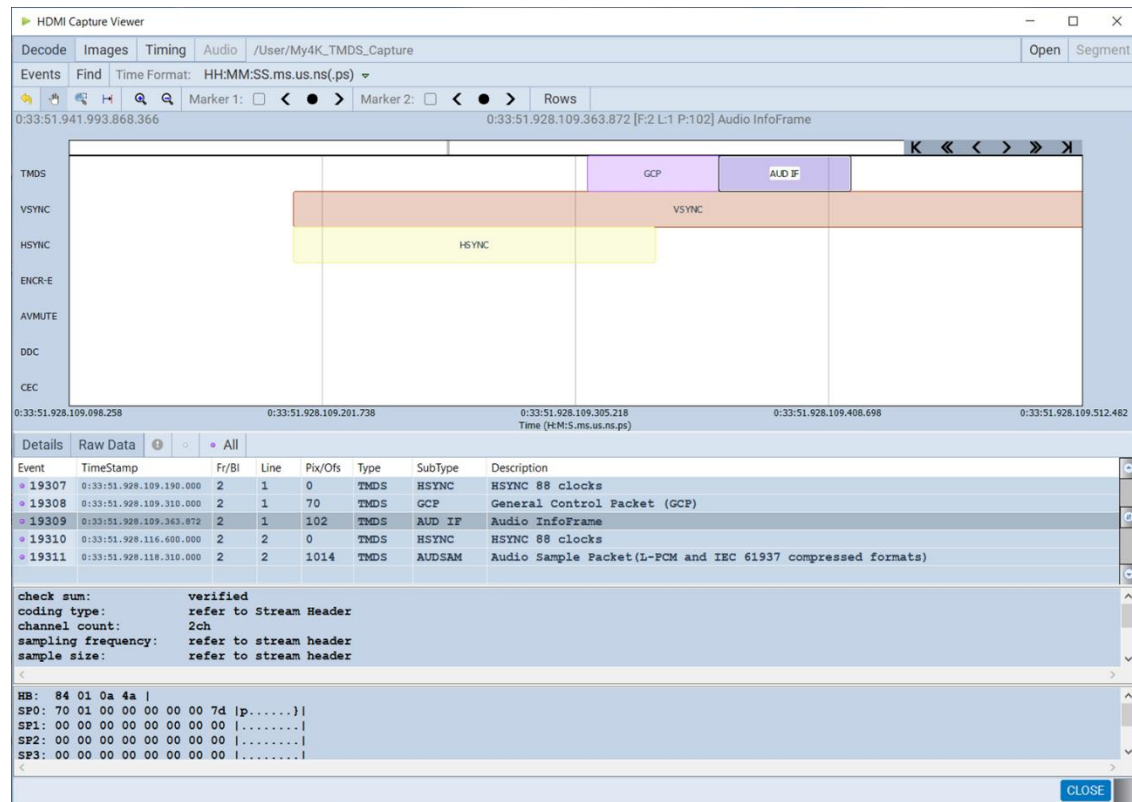
- ◆ Provides graphical view of video, audio, protocol elements in a timeline and in table form.
- ◆ Shows details of all video and protocol elements.
- ◆ Assigns precise timestamps to video / protocol elements.
- ◆ Zoom in and out to get high view or specific view.
- ◆ Provides view of embedded TMDs captured data.
- ◆ Supports searching & filtering of data.
- ◆ Enables export of capture data for sharing with colleagues.
- ◆ View captured video frames.



# HDMI TMDS Protocol Capture Analysis

## ◆ HDMI TMDS Capture & Store for Protocol Analysis:

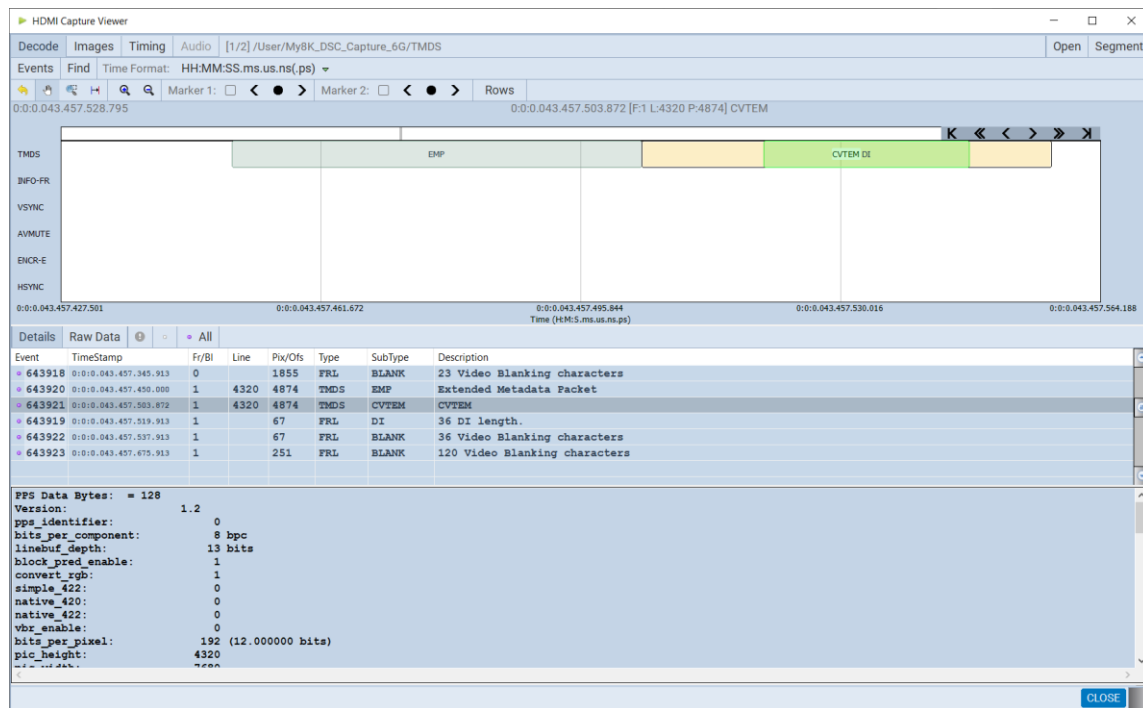
- ◆ Depicts graphical view of video, audio & protocol elements in a timeline.
- ◆ TMDS Capture shows details of all video & metadata elements.
- ◆ Protocol Capture view shows details of low level protocol such as guard bands and preambles.
- ◆ You can zoom in / out to get a high level view or specific view.
- ◆ Assigns precise timestamps to video / protocol elements.
- ◆ Supports search and filtering.
- ◆ Enables export of capture data for sharing with colleagues.



# HDMI TMDS Protocol Capture Analysis - DSC

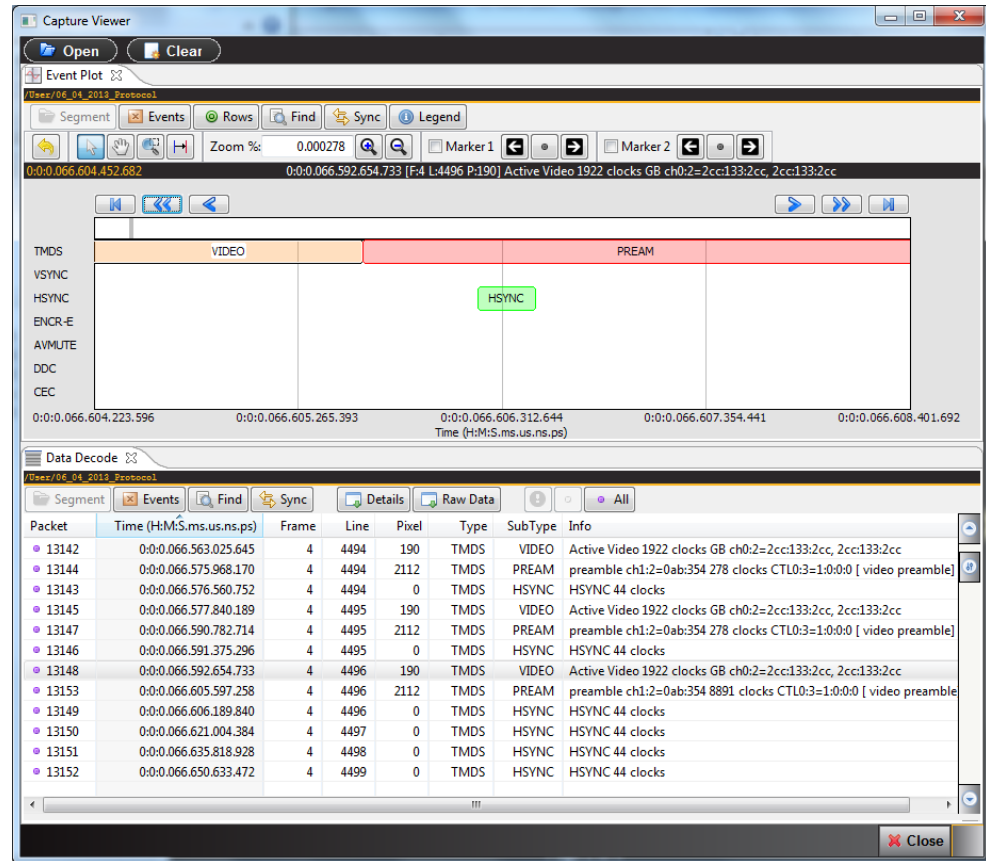
## ◆ HDMI TMDS Capture & Store for Protocol Analysis:

- ◆ Depicts graphical view of video, audio & protocol elements in a timeline.
- ◆ TMDS DSC Capture shows details of the video & the DSC metadata, the Picture Parameter Set (PPS) indicated as the CVTEM packet (right).



# HDMI TMDS Protocol Capture Analysis

- ◆ HDMI TMDS Capture & Store for Protocol Analysis:
  - ◆ Depicts graphical view of video, audio & protocol elements in a timeline.
  - ◆ TMDS Capture shows details of all video & metadata elements.
  - ◆ Protocol Capture view shows details of low level protocol such as guard bands and preambles.
  - ◆ You can zoom in / out to get a high level view or specific view.
  - ◆ Assigns precise timestamps to video / protocol elements.
  - ◆ Supports search and filtering.
  - ◆ Enables export of capture data for sharing with colleagues.
  - ◆ Timing analyzer shows Line and Frame timing parameters.





# HDMI TMDS Protocol Capture Analysis

## ◆ HDMI TMDS Capture & Store for Protocol Analysis:

- ◆ Depicts graphical view of video, audio & protocol elements in a timeline.
- ◆ TMDS Capture shows details of all video & metadata elements.
- ◆ Protocol Capture view shows details of low level protocol such as guard bands and preambles.
- ◆ You can zoom in / out to get a high level view or specific view.
- ◆ Assigns precise timestamps to video / protocol elements.
- ◆ Supports search and filtering.
- ◆ Enables export of capture data for sharing with colleagues.
- ◆ Timing analyzer shows Line and Frame timing parameters.

The screenshot displays the 'HDMI Capture Viewer' application. It features a top menu bar with 'Decode', 'Images', 'Timing', 'Audio', and a file path '/User/TMDS\_4K'. Below the menu is a 'Frame Stats' tab, which is active, showing a 'Video Format' table. This table lists parameters such as Format (2160p60), VIC (97), BPP (24), HF (135.0), I/P (P), HTotal (4400), Vtotal (2250), Hactive (3840), HS-F (176), HS-W (88), VActive (2160), VS-F (8), VS-W (4400), HS-P (Pos), VS-P (Pos), HTov (0), and PF (594.0). Below the video format is a 'Frame Statistics' table with columns for CTA Name, Frame, TimeStamp, Duration, VF Hz, HF kHz, Vtotal, Vactive, PF MHz, HS-W, VSync, Start Vid, HTov, Encr Start, Encr Len, Vfront, and Vback. It lists five frames of 3840x2160p @ 59.94Hz/60Hz. At the bottom is a 'Line Statistics' table with columns for Frame, Line, TimeStamp, Duration, HTotal, TMDS HTotal, HSync Width, HBack, and HActive. It lists lines 000 through 018. A 'Sync' button is located at the bottom right of the line statistics table.

Format	VIC	BPP	HF (kHz)	I/P	HTotal	Vtotal	Hactive	HS-F	HS-W	VActive	VS-F	VS-W	HS-P	VS-P	HTov	PF (MHz)
2160p60	97	24	135.0	P	4400	2250	3840	176	88	2160	8	4400	Pos	Pos	0	594.0

CTA Name	Frame	TimeStamp	Duration	VF Hz	HF kHz	Vtotal	Vactive	PF MHz	HS-W	VSync	Start Vid	HTov	Encr Start	Encr Len	Vfront	Vback
3840x2160p @ 59.94Hz/60Hz	0	0:17:34.618.652.430	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72
3840x2160p @ 59.94Hz/60Hz	1	0:17:34.635.319.095	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72
3840x2160p @ 59.94Hz/60Hz	2	0:17:34.651.985.763	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72
3840x2160p @ 59.94Hz/60Hz	3	0:17:34.668.652.430	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72
3840x2160p @ 59.94Hz/60Hz	4	0:17:34.685.319.095	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72
3840x2160p @ 59.94Hz/60Hz	5	0:17:34.701.985.763	0:0:0.016.666.000	60.00	135.00	2250	2160	594.000	88	10	82	0	0	0	8	72

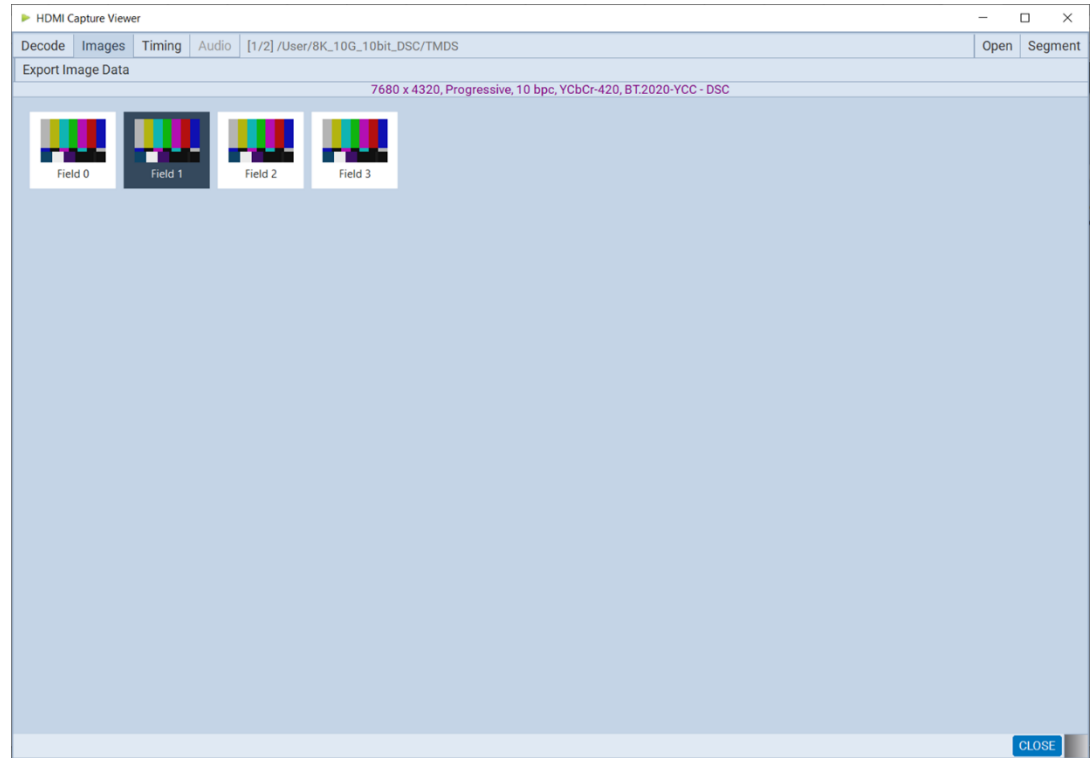
Frame	Line	TimeStamp	Duration	HTotal	TMDS HTotal	HSync Width	HBack	HActive
2	000	0:17:34.651.985.762	0:0:0.000.007.408	4400	4400	88	0	0
2	001	0:17:34.651.993.170	0:0:0.000.007.407	4400	4400	88	0	0
2	002	0:17:34.652.000.577	0:0:0.000.007.408	4400	4400	88	0	0
2	003	0:17:34.652.007.985	0:0:0.000.007.408	4400	4400	88	0	0
2	004	0:17:34.652.015.392	0:0:0.000.007.408	4400	4400	88	0	0
2	005	0:17:34.652.022.800	0:0:0.000.007.407	4400	4400	88	0	0
2	006	0:17:34.652.030.207	0:0:0.000.007.408	4400	4400	88	0	0
2	007	0:17:34.652.037.615	0:0:0.000.007.408	4400	4400	88	0	0
2	008	0:17:34.652.045.022	0:0:0.000.007.408	4400	4400	88	0	0
2	009	0:17:34.652.052.430	0:0:0.000.007.407	4400	4400	88	0	0
2	010	0:17:34.652.059.837	0:0:0.000.007.408	4400	4400	88	0	0
2	011	0:17:34.652.067.245	0:0:0.000.007.405	4400	4400	88	0	0
2	012	0:17:34.652.074.650	0:0:0.000.007.408	4400	4400	88	0	0
2	013	0:17:34.652.082.057	0:0:0.000.007.408	4400	4400	88	0	0
2	014	0:17:34.652.089.465	0:0:0.000.007.408	4400	4400	88	0	0
2	015	0:17:34.652.096.872	0:0:0.000.007.407	4400	4400	88	0	0
2	016	0:17:34.652.104.280	0:0:0.000.007.408	4400	4400	88	0	0
2	017	0:17:34.652.111.687	0:0:0.000.007.408	4400	4400	88	0	0
2	018	0:17:34.652.119.095	0:0:0.000.007.408	4400	4400	88	0	0



# HDMI Capture Viewer – View Captured Video Frames

## ◆ HDMI Capture Viewer Video Frames:

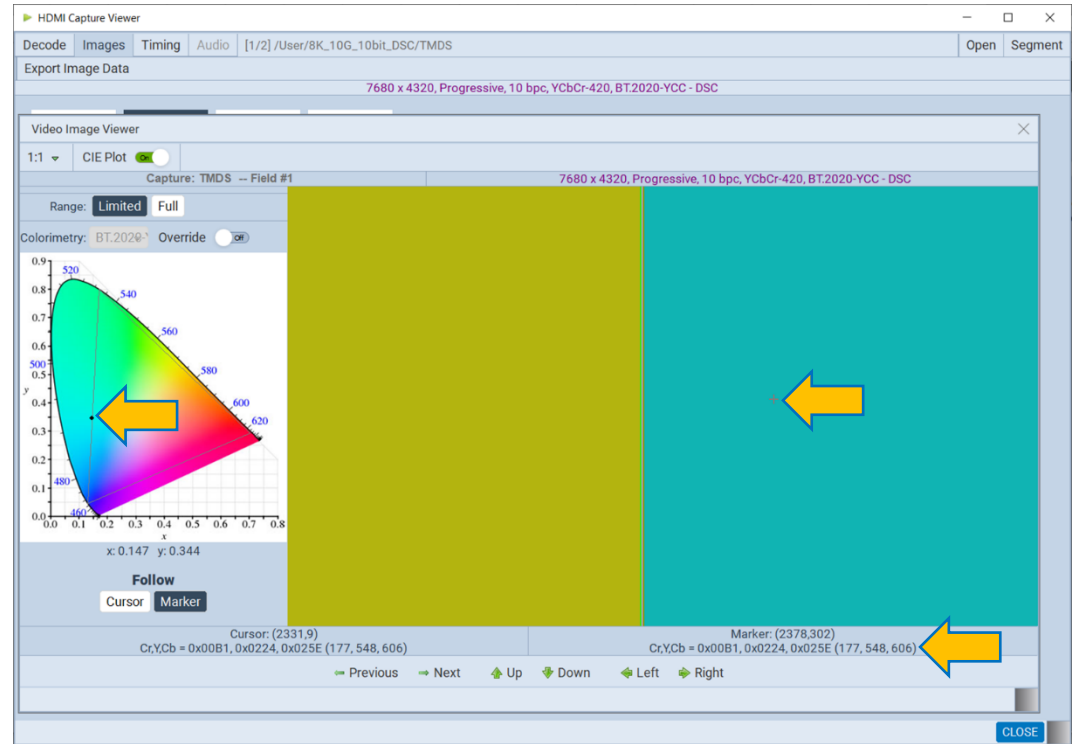
- ◆ View capture video frames to check for artifacts.



# HDMI Capture Viewer – View Captured Video Frames

## ◆ HDMI Capture Viewer Video Frames:

- ◆ View capture video frames to check for artifacts.
- ◆ Verify colorimetry parameters.
- ◆ View pixel values.
- ◆ Check colors against CIE chart.



# HDMI Capture Viewer - Searching and Filtering

- ◆ HDMI Capture Viewer Searching and Filtering:
  - ◆ Filter view to show only specific protocol or control elements (example shows audio packets).
  - ◆ View number of packets of each element type for quick at a glance insight into the integrity of the capture.

The screenshot displays the HDMI Capture Viewer application. The top toolbar includes buttons for Decode, Import, Export, and Audio, along with a file path. Below this is a search bar and a format dropdown set to 'HH:MM:SS.ms.us.ns(ps)'. A timeline at the top shows a waveform with a yellow arrow pointing to a specific section. The main area is divided into lanes for TMDs, VSYNC, HSYNC, ENCR-E, AVMUTE, DDC, and CEC. A detailed event list is shown at the bottom, with columns for Event, TimeStamp, Fr/Bi, Line, Pix/Ofs, Type, SubType, and Description. A 'Decode Event Selection' dialog box is open, showing a list of events with checkboxes for selection. A yellow arrow points to the 'Audio Sample (3861)' event in the list.

Event	TimeStamp	Fr/Bi	Line	Pix/Ofs	Type	SubType	Description
38470	0:17:34.682.259.610.000	4	1837	4262	TMDs	AUDSAM	Audio Sample Pac
38477	0:17:34.682.281.830.000	4	1840	4262	TMDs	AUDSAM	Audio Sample Pac
38484	0:17:34.682.304.050.000	4	1843	4262	TMDs	AUDSAM	Audio Sample Pac
38489	0:17:34.682.318.860.000	4	1845	4262	TMDs	AUDSAM	Audio Sample Pac
38496	0:17:34.682.341.090.000	4	1848	4262	TMDs	AUDSAM	Audio Sample Pac
38503	0:17:34.682.363.310.000	4	1851	4262	TMDs	AUDSAM	Audio Sample Pac
38510	0:17:34.682.385.530.000	4	1854	4262	TMDs	AUDSAM	Audio Sample Pac
38517	0:17:34.682.407.750.000	4	1857	4262	TMDs	AUDSAM	Audio Sample Pac
38523	0:17:34.682.422.940.000	4	1860	86	TMDs	AUDSAM	Audio Sample Pac

# HDMI Capture Viewer - Searching and Filtering

## ◆ HDMI Capture Viewer Searching and Filtering:

- ◆ Filter view to show only specific protocol or control elements (example shows audio packets).
- ◆ Search for any type of video, protocol or control element (example shows searching for a variety of HDMI FRL packets.)
- ◆ View number of packets of each element type for quick at a glance insight into the integrity of the capture.

The screenshot displays the HDMI Capture Viewer software interface. The main window shows a timeline of events with various colored bars representing different data types. A yellow arrow points to the 'Decode Event Selection' window, which is open over the timeline. This window allows users to filter events by category and type.

**Decode Event Selection**

Category	Events
Misc (0)	<input checked="" type="checkbox"/> Link Rate (1)
Packets (0)	<input checked="" type="checkbox"/> Super Block (37662)
InfoFrame (0)	<input checked="" type="checkbox"/> Character Block (150646)
Control (0)	<input checked="" type="checkbox"/> Gap (1439479)
DDC (0)	<input checked="" type="checkbox"/> Active (1316466)
FRL (3145728)	<input checked="" type="checkbox"/> Blank (26347)
Other (0)	<input checked="" type="checkbox"/> FEC Parity (150645)
	<input checked="" type="checkbox"/> FEC Error (0)
	<input checked="" type="checkbox"/> Error (0)

Additional filters on the right side of the window include:

- ☒ H-Sync (8023)
- ☒ V-Sync (771)
- ☒ Encryption Enable (0)
- ☒ Video Preamble (4500)
- ☒ Video Guard Band (4496)
- ☒ Data Island (1673)
- ☒ DI Preamble (1673)
- ☒ DI Leading GB (1673)
- ☒ DI Trailing GB (1673)

Buttons at the bottom: SELECT ALL CATEGORIES & EVENTS, CLEAR ALL CATEGORIES & EVENTS, OK, CANCEL.

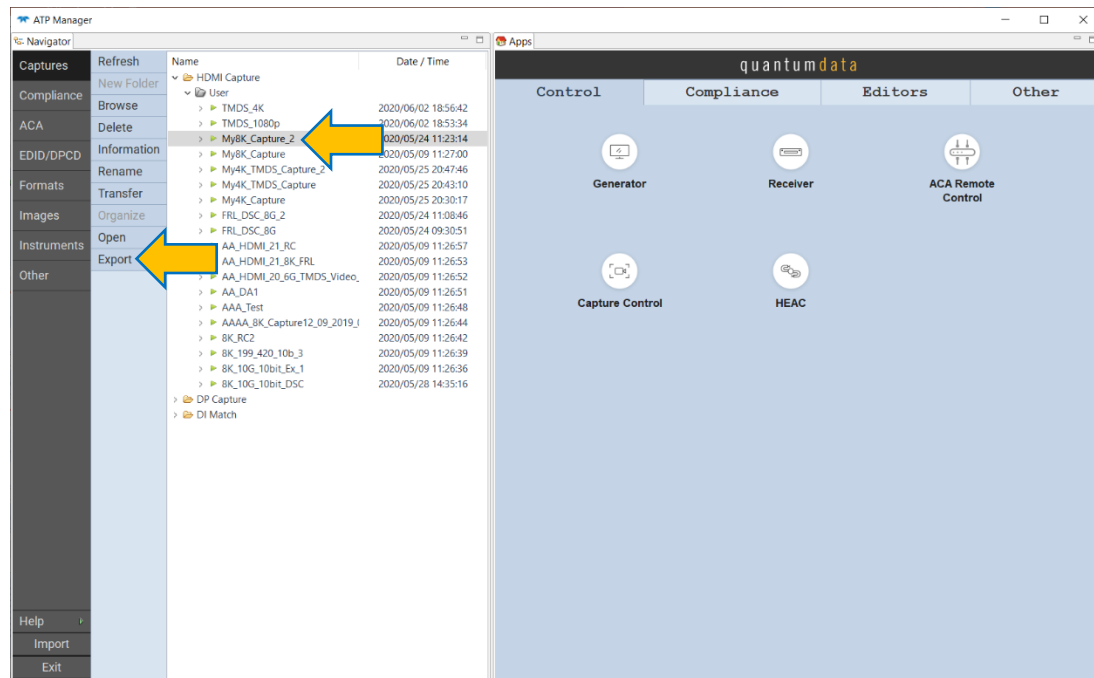




# HDMI Capture Viewer – Export Capture Data

## ◆ HDMI Capture Viewer Export:

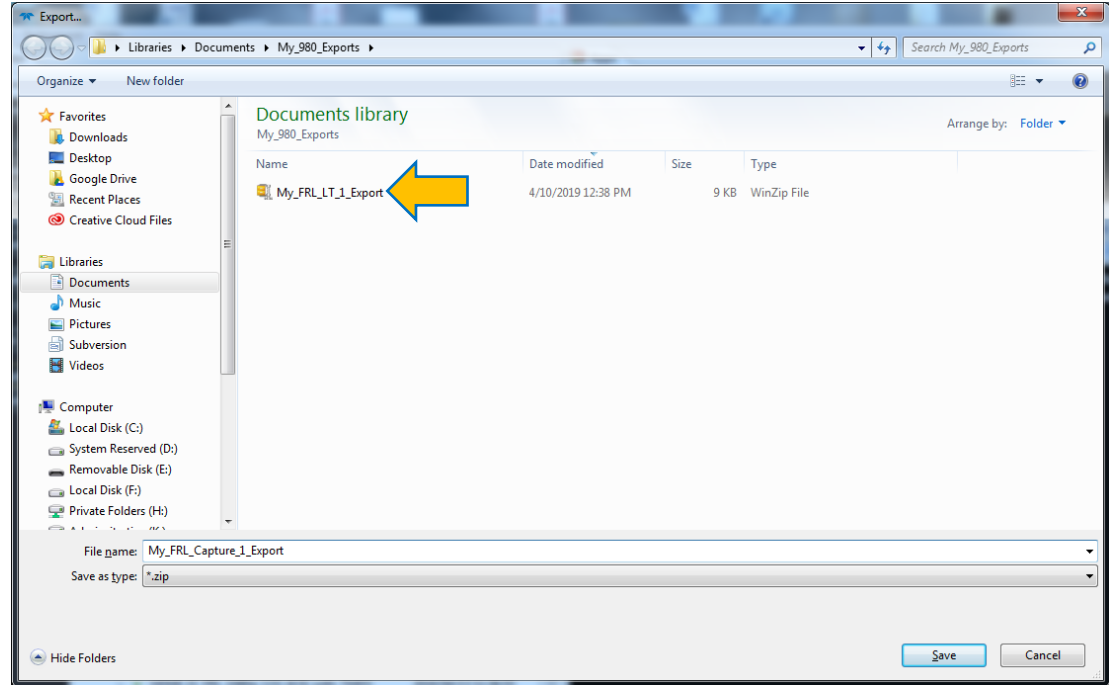
- ◆ Export capture data to disseminate to colleagues, other subject matter experts or Teledyne Customer Support.
- ◆ Exported capture does not require an 980 48G module instrument to view; viewing exported/imported capture only requires ATP Manager which is available on the quantumdata website.



# HDMI Capture Viewer – Export Capture Data

## ◆ HDMI Capture Viewer Export:

- ◆ Export capture data to disseminate to colleagues, other subject matter experts or Teledyne Customer Support.
- ◆ Exported capture does not require an 980 48G module instrument to view; viewing exported/imported capture only requires ATP Manager which is available on the quantumdata website.
- ◆ Transfer to PC to save and recall later for analysis.



# HDMI Sink Emulation – Emulate EDIDs and Sink Capability Registers

## ◆ HDMI EDID and Register Emulation:

- ◆ Create custom EDIDs with the EDID Editor for emulation and verify source response to changing video parameters.
- ◆ Create custom HDMI SCDC register values for emulation and verify source response to link configurations.

The screenshot shows the EDID Editor application window. The left sidebar contains a tree view with the following structure:

- Base Block
  - Header
  - Vendor/Product Information
  - EDID Version/Revision
  - Basic Display Parameters/Features
    - Color Characteristics
    - Established Timings
    - Standard Timings
    - Descriptor 1
    - Descriptor 2
    - Descriptor 3
    - Descriptor 4
    - Extension Flag
    - Checksum
- CTA Block
  - Header
  - Data Blocks
    - Video Data
    - Audio Data
    - Vendor Specific HDMI 1.4b (selected)
    - Vendor Specific HDMI Forum
    - Video Capability
    - Speaker Allocation
    - YCbCr 4:2:0 Capability Map
    - YCbCr 4:2:0 Video Data
    - HDR Static Metadata
    - Colorimetry
  - Detailed Timing Descriptors
  - Checksum

The main area displays the configuration for the selected 'Vendor Specific HDMI 1.4b' block. It includes fields for IEEE OUI (000C03), Components of Source Physical Address (1, 0, 0, 0, 0, 0), and various checkboxes for supported features like ACP, ISRC, 48/36 bits/pixel, YCbCr 4:4:4, and CNC0-3. The Maximum TMDs Clock rate is set to 340 MHz. Below these are tabs for Audio/Video Latency and HDMI Video/3D. The Audio/Video Latency tab is active, showing fields for Video Latency, Audio Latency, Interlaced Video Latency, and Interlaced Audio Latency, each with a dropdown menu. At the bottom, there is a hex dump of the block data, with the first 128 bytes displayed in two columns.

Block 1: 128 bytes																Element: Offset = 34, Length = 25															
02	03	5F	F0	59	10	05	20	22	04	03	02	07	14	78	03	0C	00	10	00	F8	44	2F	C8	8A	01	02	14				
5F	60	61	62	64	65	66	C2	C4	C3	76	75	7E	7F	41	00	16	06	08	00	56	58	00	6D	D8	83	81					
04	81	41	00	16	06	08	00	56	58	00	6D	D8	83	81	41	00	16	06	08	00	56	58	00	6D	D8	83					
78	88	47	00	00	00	CF	47	3F	E2	00	48	83	E1	0F	E4	0E	C7	C6	C5	E3	06	0F	01	E3	05						
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						



# HDMI DDC Source Testing Aux Channel Analyzer

# Aux Channel Analyzer (ACA) – HDMI FRL Link Training

- ◆ HDMI Aux Channel Analyzer (ACA) for DDC monitoring:
  - ◆ Enables monitoring and analysis of the HDMI connection sequence.
  - ◆ Verify EDID exchange, HDCP authentication (not shown).
  - ◆ View FRL link training transactions.
  - ◆ Assigns precise timestamps for each transaction; provides user controls to associate events.
  - ◆ Supports search and filtering functions.
  - ◆ Enables export of transaction logs to share with colleagues.

ACA Data Viewer

Open Close Export Options Filter Find

Events: 129 (129)

Line	Transaction	Timestamp	Data Rate
16	SCDC HDMI-R30	+00:43:56.475016	< 43 (48.67 kbps)
17	SCDCV HDMI-R30	+00:43:56.477637	Update Reads 102: 43
18	SCDC HDMI-R30	+00:43:58.797904	Address 0xA8 NACKed
19	EDID HDMI-R30	+00:43:58.847711	W Segment 00 (48.67 kbps)
20	EDID HDMI-R30	+00:43:58.848202	R EDID 00 (48.67 kbps)
21	EDID HDMI-R30	+00:43:58.848530	< 128 bytes (48.67 kbps)
22	EDID HDMI-R30	+00:43:58.978617	W Segment 00 (48.67 kbps)
23	EDID HDMI-R30	+00:43:58.979108	R EDID 80 (48.67 kbps)
24	EDID HDMI-R30	+00:43:58.979436	< 128 bytes (48.67 kbps)
25	SCDC HDMI-R30	+00:43:59.060863	R Sink Version (48.67 kbps)
26	SCDC HDMI-R30	+00:43:59.061355	< 01 (48.67 kbps)
27	SCDC HDMI-R30	+00:43:59.061683	W Source Version 01 (48.67 kbps)
28	SCDC HDMI-R30	+00:43:59.062502	R Status_Flags_0 (48.67 kbps)
29	SCDC HDMI-R30	+00:43:59.062993	< 41 (48.67 kbps)
30	SCDC HDMI-R30	+00:43:59.068400	W Config 1 06 (48.67 kbps)
31	SCDC HDMI-R30	+00:43:59.069055	W Config 0 00 (48.67 kbps)
32	SCDC HDMI-R30	+00:43:59.069711	R Update_0 (48.67 kbps)
33	SCDC HDMI-R30	+00:43:59.070202	< 01 (48.67 kbps)
34	SCDC HDMI-R30	+00:43:59.072660	R Update_0 (48.67 kbps)
35	SCDC HDMI-R30	+00:43:59.073151	< 01 (48.67 kbps)
36	SCDC HDMI-R30	+00:43:59.076100	R Update_0 (48.67 kbps)
37	SCDC HDMI-R30	+00:43:59.076428	< 63 (48.67 kbps)
38	SCDC HDMI-R30	+00:43:59.076919	R Status_Flags_1 (48.67 kbps)
39	SCDC HDMI-R30	+00:43:59.077247	< 65 (48.67 kbps)
40	SCDC HDMI-R30	+00:43:59.077739	R Status_Flags_2 (48.67 kbps)
41	SCDC HDMI-R30	+00:43:59.078230	< 87 (48.67 kbps)
42	SCDC HDMI-R30	+00:43:59.078722	R Update_0 (48.67 kbps)
43	SCDC HDMI-R30	+00:43:59.079049	< 63 (48.67 kbps)
44	SCDC HDMI-R30	+00:43:59.079541	W Update_0 63 (48.67 kbps)
45	SCDC HDMI-R30	+00:43:59.082326	R Update_0 (48.67 kbps)
46	SCDC HDMI-R30	+00:43:59.082654	< 00 (48.67 kbps)
47	SCDCV HDMI-R30	+00:43:59.085111	Update Reads 52: 00
48	SCDC HDMI-R30	+00:43:59.232893	R Update_0 (48.67 kbps)
49	SCDC HDMI-R30	+00:43:59.233384	< 21 (48.67 kbps)

Type: SCDC  
Start Time: +00:43:59.068400  
Duration: 328 to 452 us  
Maximum I2C Rate: 48.67 kbps  
Write, 1 byte  
31h: Config\_1

Bit Name	Value	Description
3-0 FRL_Rate	6	FRL, 12 Gps/lane, 4 Lanes
7-4 FFE_Levels	0	

\* START \*  
0000 A8 31 06 | . 1 .  
\* STOP \*

30: W Config 1 06 (48.67 kbps)



# Aux Channel Analyzer (ACA) – HDMI FRL Link Training

## ◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Save ACA log as an HTML file.
- ◆ Export capture data to disseminate to colleagues, other subject matter experts or Teledyne Customer Support.
- ◆ Exported capture does not require 980 48G module instrument; only requires ATP Manager.
- ◆ Transfer to PC to save and recall later for analysis.

The screenshot displays the ACA Data Viewer application. The main window is titled 'ACA Data Viewer' and contains a menu bar with 'Open', 'Close', 'Export', 'Options', 'Filter', and 'Find'. Below the menu bar is a tab labeled '[AAA\_HDMI\_48G\_FRL\_LT] Events: 129 (129)'. The main area is a list of events, each with a line number, a type (SCDC), a channel (HDMI-R30), a timestamp, and a description. The events are sorted by timestamp. A yellow arrow points to the event at line 77, which is 'SCDC HDMI-R30 +00:43:59.305145 < 00 (48.67 kbps)'. To the right of the event list is a detailed view of the selected event. It shows the 'Type: SCDC', 'Start Time: +00:43:59.305145', 'Duration: 328 to 492 us', 'Maximum I2C Rate: 48.67 kbps', and 'Read, 1 byte'. Below this is a table titled '41h: Status\_Flags\_1' with columns 'Bit', 'Name', 'Value', and 'Description'. The table has two rows: '3-0 In0\_LTF\_req' with value '0' and description 'No Pattern Requested', and '7-4 In1\_LTF\_req' with value '0' and description 'No Pattern Requested'. A yellow arrow points to the 'Value' column of the second row. At the bottom of the detailed view, there is a section for 'START' and 'STOP' markers, with 'START' at '0000 A9 00-' and 'STOP' at 'STOP \*'. A yellow arrow points to the 'STOP' marker.

Bit	Name	Value	Description
3-0	In0_LTF_req	0	No Pattern Requested
7-4	In1_LTF_req	0	No Pattern Requested

# Aux Channel Analyzer (ACA) – HDCP 2.3 Authentication

- ◆ HDMI Aux Channel Analyzer (ACA) for DDC monitoring:
  - ◆ Enables monitoring and analysis of the HDMI connection sequence.
  - ◆ Verify EDID exchange, HDCP authentication.

ACA Data Viewer

Open Close Export Options Filter Find

[ACMT\_HDCP\_1B\_07\_2] Events: 1078 (1078)

Line	Protocol	Direction	Time	Event	Speed
120	HDCP	HDMI-R10	+00:49:31.876756	R RxStatus (73.91 kbps)	< 0000 (82.33 kbps)
121	HDCP	HDMI-R10	+00:49:31.877084	W Segment 00 (73.80 kbps)	R EDID 00 (73.80 kbps)
122	EDID	HDMI-R10	+00:49:32.368433	< 128 bytes (82.61 kbps)	W Segment 00 (73.80 kbps)
123	EDID	HDMI-R10	+00:49:32.368597	R EDID 00 (73.80 kbps)	< 128 bytes (82.61 kbps)
124	EDID	HDMI-R10	+00:49:32.368924	W Segment 00 (73.80 kbps)	R EDID 80 (73.80 kbps)
125	EDID	HDMI-R10	+00:49:32.399562	W Segment 00 (73.80 kbps)	< 128 bytes (82.61 kbps)
126	EDID	HDMI-R10	+00:49:32.399890	R EDID 80 (73.80 kbps)	< 04 (82.33 kbps)
127	EDID	HDMI-R10	+00:49:32.400217	R HDCP2Version (73.69 kbps)	R RxStatus (73.80 kbps)
128	HDCP	HDMI-R10	+00:49:36.027743	< 04 (82.33 kbps)	< 0000 (82.33 kbps)
129	HDCP	HDMI-R10	+00:49:36.028071	R RxStatus (73.80 kbps)	W AKE_Init (73.91 kbps)
130	HDCP	HDMI-R10	+00:49:36.033641	R RxStatus (73.80 kbps)	R RxStatus (73.80 kbps)
131	HDCP	HDMI-R10	+00:49:36.033805	< 0000 (82.33 kbps)	< 1602 (82.47 kbps)
132	HDCP	HDMI-R10	+00:49:36.040850	W AKE_Init (73.91 kbps)	R Read_Message (73.80 kbps)
133	HDCP	HDMI-R10	+00:49:36.096719	R RxStatus (73.80 kbps)	< AKE_Send_Cert (82.61 kbps)
134	HDCP	HDMI-R10	+00:49:36.096883	< 1602 (82.47 kbps)	W AKE_No_Stored_km (73.91 kbps)
135	HDCP	HDMI-R10	+00:49:36.097702	R Read_Message (73.80 kbps)	R RxStatus (73.80 kbps)
136	HDCP	HDMI-R10	+00:49:36.098030	< AKE_Send_Cert (82.61 kbps)	< 2100 (82.47 kbps)
137	HDCP	HDMI-R10	+00:49:36.349029	W AKE_No_Stored_km (73.91 kbps)	R Read_Message (73.80 kbps)
138	HDCP	HDMI-R10	+00:49:36.565786	R RxStatus (73.80 kbps)	< AKE_Send_H_prime (82.47 kbps)
139	HDCP	HDMI-R10	+00:49:36.566113	< 2100 (82.47 kbps)	R RxStatus (73.80 kbps)
140	HDCP	HDMI-R10	+00:49:36.566933	R Read_Message (73.80 kbps)	< 1100 (82.47 kbps)
141	HDCP	HDMI-R10	+00:49:36.567260	< AKE_Send_H_prime (82.47 kbps)	R Read_Message (73.80 kbps)
142	HDCP	HDMI-R10	+00:49:36.621490	R RxStatus (73.80 kbps)	< AKE_Send_Pairing_Info (82.47 kbps)
143	HDCP	HDMI-R10	+00:49:36.621818	< 1100 (82.47 kbps)	W LC_Init (73.80 kbps)
144	HDCP	HDMI-R10	+00:49:36.622637	R Read_Message (73.80 kbps)	R RxStatus (73.69 kbps)
145	HDCP	HDMI-R10	+00:49:36.622965	< AKE_Send_Pairing_Info (82.47 kbps)	< 2100 (82.47 kbps)
146	HDCP	HDMI-R10	+00:49:36.637219	W LC_Init (73.80 kbps)	R Read_Message (73.80 kbps)
147	HDCP	HDMI-R10	+00:49:36.659173	R RxStatus (73.69 kbps)	< LC_Send_L_prime (82.47 kbps)
148	HDCP	HDMI-R10	+00:49:36.659337	< 2100 (82.47 kbps)	W SKE_Send_Eks (73.91 kbps)
149	HDCP	HDMI-R10	+00:49:36.660156	R Read_Message (73.80 kbps)	R RxStatus (73.80 kbps)
150	HDCP	HDMI-R10	+00:49:36.660484	< LC_Send_L_prime (82.47 kbps)	< 0000 (82.47 kbps)
151	HDCP	HDMI-R10	+00:49:36.672280	W SKE_Send_Eks (73.91 kbps)	R RxStatus (73.69 kbps)
152	HDCP	HDMI-R10	+00:49:36.879371	R RxStatus (73.80 kbps)	< 0000 (82.47 kbps)
153	HDCP	HDMI-R10	+00:49:36.879698	< 0000 (82.47 kbps)	R RxStatus (73.69 kbps)
154	HDCP	HDMI-R10	+00:49:37.080563	R RxStatus (73.69 kbps)	< 0000 (82.47 kbps)
155	HDCP	HDMI-R10	+00:49:37.080727	< 0000 (82.47 kbps)	R RxStatus (73.80 kbps)
156	HDCP	HDMI-R10	+00:49:37.281592	R RxStatus (73.80 kbps)	

Type: HDCP

Start Time: +00:49:36.098030

Duration: 58.982 msec

Maximum I2C Rate: 82.61 kbps

Read, 534 bytes

Register: 80h

Name: Read\_Message

Message: AKE\_Send\_Cert (534 bytes)

msg\_id: 3

cert\_tx:[4175..0]

Receiver ID: 8C 23 BA D5 A6

Receiver Public Key:

C5 3B FC EC 4E 2A 42 EA 71 76 F4 B8 90 7A EC

F5 78 07 11 97 35 5C D6 F8 09 30 D3 DB 4C 91

7D 82 CE F6 7D 7F 22 A1 1D A7 9F 6F C1 4A 52

AE 09 5A CC 59 FD 5F C2 07 19 D8 A7 02 D0 4C

B8 16 F4 DA 3A 12 B8 00 84 E1 D3 2E 2C EA 76

83 F8 12 B0 74 E6 B9 CB 5B BD BB F8 39 A3 26

DF B9 E9 5A BD 0F 97 89 73 63 38 2B 95 1D 52

CA 1F 07 46 F1 14 36 1A 3F 61 BE 2E C2 E2 75

01 00 01

RESERVED: 00 00

DCP LLC Signature:

28 A8 50 53 80 72 16 76 A3 EB 07 D7 FC F7 A7

38 72 33 D5 26 76 87 64 3A D1 A4 45 45 86 6D

90 58 B4 3E 16 CD B8 B7 24 D7 74 F9 4E 76 C5

1B D0 B8 4B 53 33 1A 60 72 E2 3A 8A 79 FE BC

52 9C 21 8E 4D 9F 8A 33 2E BA 8F B4 69 36 C4

DF B9 E9 5A BD 0F 97 89 73 63 38 2B 95 1D 52

4A DF 57 82 1F 03 23 DB DB 41 0B 25 79 28 FE

72 ED 4D 42 1F D8 7F 31 A4 9A 97 97 8E 13 10

0D 00 EB 48 97 71 5E 5C B5 1A F1 86 60 0D BA

CC 9A 2C 40 B8 1B 59 50 7B 2A 0B 46 EF DE C3

FF 8E AD E7 9A 0E FC D2 D2 1C 9E 35 25 5E 2C

F7 CC 4C FE B2 0E C2 56 46 57 9F F5 1A 32

5E E1 58 12 57 48 47 33 96 4C 0B 99 E7 C3 5E

61 20 DD B6 23 BE 3E 97 82 4F 11 B4 70 86 2F

A8 C2 95 C1 F5 EC 39 8F EC E3 7E FD 01 36 EE

B2 F0 95 01 A4 74 92 F5 3C 10 9B 5B B9 60 61

BC 5E 0C 07 DA 72 C7 74 B6 15 75 B1 65 A7 BF

88 E7 F0 D9 16 9E 13 D5 8D 96 93 0F 3A E1 0D

136: < AKE\_Send\_Cert (82.61 kbps)

# Aux Channel Analyzer (ACA) – HDCP 2.3 Authentication

- ◆ HDMI Aux Channel Analyzer (ACA) for DDC monitoring:
  - ◆ Enables monitoring and analysis of the HDMI connection sequence.
  - ◆ Verify EDID exchange, HDCP authentication.

ACA Data Viewer

Open Close Export Options Filter Find

[ACMT\_HDCP\_TB\_07\_2] Events: 1078 (1078)

Line	Protocol	Channel	Time	Event	Rate
120	HDCP	HDMI-R10	+00:49:31.876756	R RxStatus	(73.91 kbps)
121	HDCP	HDMI-R10	+00:49:31.877084	< 0000	(82.33 kbps)
122	EDID	HDMI-R10	+00:49:32.368433	W Segment 00	(73.80 kbps)
123	EDID	HDMI-R10	+00:49:32.368597	R EDID 00	(73.80 kbps)
124	EDID	HDMI-R10	+00:49:32.368924	< 128 bytes	(82.61 kbps)
125	EDID	HDMI-R10	+00:49:32.399562	W Segment 00	(73.80 kbps)
126	EDID	HDMI-R10	+00:49:32.399890	R EDID 80	(73.80 kbps)
127	EDID	HDMI-R10	+00:49:32.400217	< 128 bytes	(82.61 kbps)
128	HDCP	HDMI-R10	+00:49:36.027743	R HDCP2Version	(73.69 kbps)
129	HDCP	HDMI-R10	+00:49:36.028071	< 04	(82.33 kbps)
130	HDCP	HDMI-R10	+00:49:36.033641	R RxStatus	(73.80 kbps)
131	HDCP	HDMI-R10	+00:49:36.033805	< 0000	(82.33 kbps)
132	HDCP	HDMI-R10	+00:49:36.040850	W AKE_Init	(73.91 kbps)
133	HDCP	HDMI-R10	+00:49:36.096719	R RxStatus	(73.80 kbps)
134	HDCP	HDMI-R10	+00:49:36.096883	< 1602	(82.47 kbps)
135	HDCP	HDMI-R10	+00:49:36.097702	R Read_Message	(73.80 kbps)
136	HDCP	HDMI-R10	+00:49:36.098030	< AKE_Send_Cert	(82.61 kbps)
137	HDCP	HDMI-R10	+00:49:36.349029	W AKE_No_Stored_km	(73.91 kbps)
138	HDCP	HDMI-R10	+00:49:36.565786	R RxStatus	(73.80 kbps)
139	HDCP	HDMI-R10	+00:49:36.566113	< 2100	(82.47 kbps)
140	HDCP	HDMI-R10	+00:49:36.566933	R Read_Message	(73.80 kbps)
141	HDCP	HDMI-R10	+00:49:36.567260	< AKE_Send_H_prime	(82.47 kbps)
142	HDCP	HDMI-R10	+00:49:36.621490	R RxStatus	(73.80 kbps)
143	HDCP	HDMI-R10	+00:49:36.621818	< 1100	(82.47 kbps)
144	HDCP	HDMI-R10	+00:49:36.622637	R Read_Message	(73.80 kbps)
145	HDCP	HDMI-R10	+00:49:36.622965	< AKE_Send_Pairing_Info	(82.47 kbps)
146	HDCP	HDMI-R10	+00:49:36.637219	W LC_Init	(73.80 kbps)
147	HDCP	HDMI-R10	+00:49:36.659173	R RxStatus	(73.69 kbps)
148	HDCP	HDMI-R10	+00:49:36.659337	< 2100	(82.47 kbps)
149	HDCP	HDMI-R10	+00:49:36.660156	R Read_Message	(73.80 kbps)
150	HDCP	HDMI-R10	+00:49:36.660484	< LC_Send_L_prime	(82.47 kbps)
151	HDCP	HDMI-R10	+00:49:36.672280	W SKE_Send_Eks	(73.91 kbps)
152	HDCP	HDMI-R10	+00:49:36.879371	R RxStatus	(73.80 kbps)
153	HDCP	HDMI-R10	+00:49:36.879698	< 0000	(82.47 kbps)
154	HDCP	HDMI-R10	+00:49:37.080563	R RxStatus	(73.69 kbps)
155	HDCP	HDMI-R10	+00:49:37.080727	< 0000	(82.47 kbps)
156	HDCP	HDMI-R10	+00:49:37.281592	R RxStatus	(73.80 kbps)

Type: HDCP  
Start Time: +00:49:36.349029  
Duration: 16.220 msec  
Maximum 12C Rate: 73.91 kbps

Write, 129 bytes  
Register: 60h  
Name: Write\_Message

Message: AKE\_No\_Stored\_km (129 bytes)  
msg\_id: 4  
Ekrpub\_km[1023..0]:  
38 51 27 27 85 36 1F B6 87 EF F1 4F F7 63 41 1A  
58 7D 7C B9 C5 34 9E DD 05 A5 F9 5B 01 3A B5 EB  
48 05 S2 11 9A C6 64 93 69 67 47 12 38 C8 10 73  
B1 89 OF D4 D8 57 75 94 B8 60 8E 90 C8 03 D0 1B  
A5 EA 83 2A 70 BC F5 CD 02 5E 32 CB 78 2C 6D 53  
B1 6E AF 58 60 9F 09 D0 E5 E1 BC C3 12 7D E2 DC  
84 DB 21 B3 91 16 C4 D8 7A 4D 9A 32 D7 DF 29 B4  
A2 D1 56 D9 FE 41 45 0E 69 AF 31 45 B3 7B 65 8C

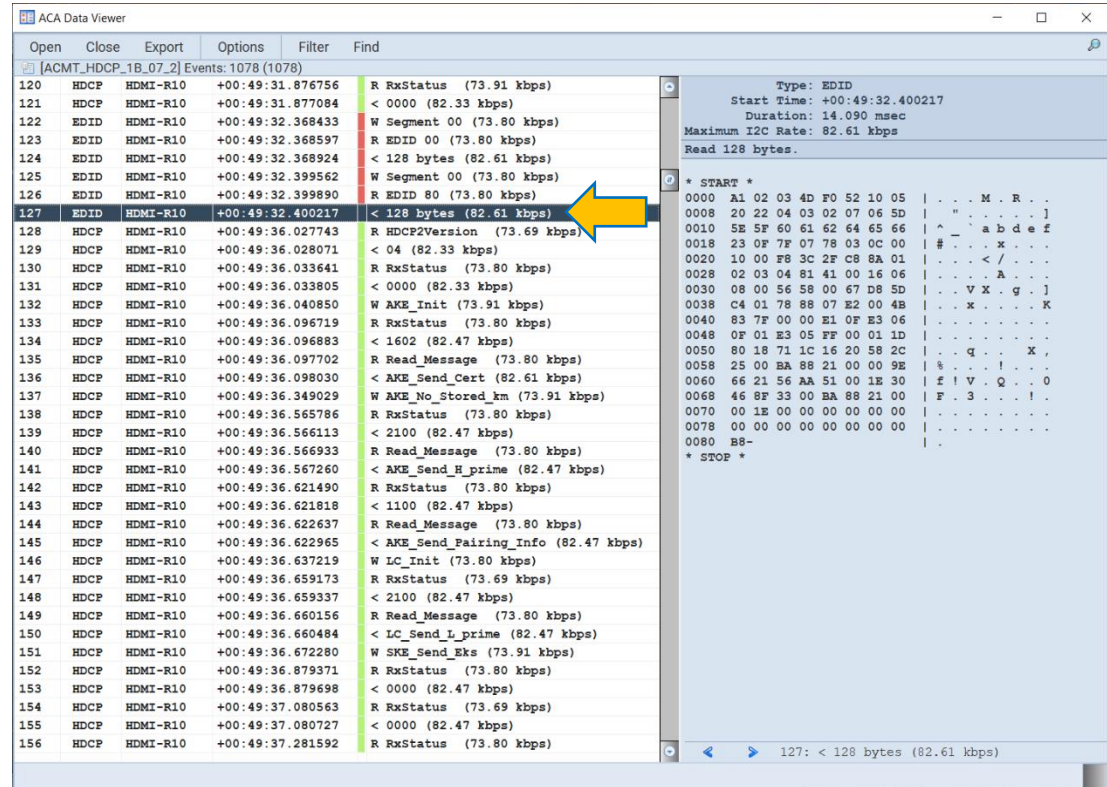
START \*  
0000 74 60 04 38 51 27 27 85 | t . . 8 Q . .  
0008 36 1F B6 87 EF F1 4F F7 | 6 . . . . . O .  
0010 63 41 1A 58 7D 7C B9 C5 | c A . X | | . .  
0018 34 9E DD 05 A5 F9 5B 01 | . . . . . [ .  
0020 3A B5 EB 48 05 52 11 9A | . . . . . H . R .  
0028 C6 64 93 69 67 47 12 3B | . d . i g G . ;  
0030 C8 10 73 B1 89 OF D4 D8 | . . . . . s .  
0038 57 75 94 B8 60 8E 90 C8 | W u . . . . .  
0040 03 D0 1B A5 EA 83 2A 70 | . . . . . \* p  
0048 EC F5 CD 02 5E 32 CB 7F | . . . . . ^ 2 .  
0050 2C 6D 53 B1 6E AF 5E 60 | . , m s n . ^ .  
0058 9F 09 D0 E5 E1 BC C3 12 | . . . . .  
0060 7D E2 DC 84 DB 21 B3 91 | . . . . . ! .  
0068 16 C4 D8 7A 4D 9A 32 D7 | . . . . . x M . 2 .  
0070 DF 29 B4 A2 D1 56 D9 FE | . . . . . V .  
0078 41 45 0E 69 AF 31 45 B3 | A E . i . 1 E .  
0080 7B 65 8C | | { e .  
\* STOP \*

137: W AKE\_No\_Stored\_km (73.91 kbps)



# Aux Channel Analyzer (ACA) – EDID Exchange HDCP 1.4

- ◆ HDMI Aux Channel Analyzer (ACA) for DDC monitoring:
  - ◆ Enables monitoring and analysis of the HDMI connection sequence.
  - ◆ Verify EDID exchange, HDCP authentication transactions.
  - ◆ Supports search and filtering functions.
  - ◆ Assigns precise timestamps for each transaction; provides user controls to associate events.
  - ◆ Enables export of transaction logs to share with colleagues.



ACA Data Viewer

Open Close Export Options Filter Find

[ACMT\_HDCP\_1B\_07\_2] Events: 1078 (1078)

120	HDCP	HDMI-R10	+00:49:31.876756	R RxStatus (73.91 kbps)	< 0000 (82.33 kbps)
121	HDCP	HDMI-R10	+00:49:31.877084	W Segment 00 (73.80 kbps)	R EDID 00 (73.80 kbps)
122	EDID	HDMI-R10	+00:49:32.368433	< 128 bytes (82.61 kbps)	W Segment 00 (73.80 kbps)
123	EDID	HDMI-R10	+00:49:32.368597	R EDID 80 (73.80 kbps)	< 128 bytes (82.61 kbps)
124	EDID	HDMI-R10	+00:49:32.368924	R RxStatus (73.80 kbps)	< 0000 (82.33 kbps)
125	EDID	HDMI-R10	+00:49:32.399562	W AKE_Init (73.91 kbps)	R RxStatus (73.80 kbps)
126	EDID	HDMI-R10	+00:49:32.399890	R RxStatus (73.80 kbps)	< 1602 (82.47 kbps)
127	EDID	HDMI-R10	+00:49:32.400217	R Read_Message (73.80 kbps)	< AKE_Send_Cert (82.61 kbps)
128	HDCP	HDMI-R10	+00:49:36.027743	W AKE_No_Stored_km (73.91 kbps)	R RxStatus (73.80 kbps)
129	HDCP	HDMI-R10	+00:49:36.028071	R RxStatus (73.80 kbps)	< 0000 (82.33 kbps)
130	HDCP	HDMI-R10	+00:49:36.033641	W AKE_Init (73.91 kbps)	R RxStatus (73.80 kbps)
131	HDCP	HDMI-R10	+00:49:36.033805	R RxStatus (73.80 kbps)	< 1602 (82.47 kbps)
132	HDCP	HDMI-R10	+00:49:36.040850	R Read_Message (73.80 kbps)	< AKE_Send_Cert (82.61 kbps)
133	HDCP	HDMI-R10	+00:49:36.096719	W AKE_No_Stored_km (73.91 kbps)	R RxStatus (73.80 kbps)
134	HDCP	HDMI-R10	+00:49:36.096883	R RxStatus (73.80 kbps)	< 2100 (82.47 kbps)
135	HDCP	HDMI-R10	+00:49:36.097702	R Read_Message (73.80 kbps)	< AKE_Send_H_prime (82.47 kbps)
136	HDCP	HDMI-R10	+00:49:36.098030	R RxStatus (73.80 kbps)	< 1100 (82.47 kbps)
137	HDCP	HDMI-R10	+00:49:36.349029	W AKE_No_Stored_km (73.91 kbps)	R RxStatus (73.80 kbps)
138	HDCP	HDMI-R10	+00:49:36.565786	R RxStatus (73.80 kbps)	< AKE_Send_Pairing_Info (82.47 kbps)
139	HDCP	HDMI-R10	+00:49:36.566113	R Read_Message (73.80 kbps)	W LC_Init (73.80 kbps)
140	HDCP	HDMI-R10	+00:49:36.566933	R RxStatus (73.80 kbps)	R RxStatus (73.69 kbps)
141	HDCP	HDMI-R10	+00:49:36.567260	< AKE_Send_H_prime (82.47 kbps)	< 2100 (82.47 kbps)
142	HDCP	HDMI-R10	+00:49:36.621490	R RxStatus (73.80 kbps)	R Read_Message (73.80 kbps)
143	HDCP	HDMI-R10	+00:49:36.621818	< 1100 (82.47 kbps)	< AKE_Send_Pairing_Info (82.47 kbps)
144	HDCP	HDMI-R10	+00:49:36.622637	R Read_Message (73.80 kbps)	W LC_Init (73.80 kbps)
145	HDCP	HDMI-R10	+00:49:36.622965	< AKE_Send_Pairing_Info (82.47 kbps)	R RxStatus (73.69 kbps)
146	HDCP	HDMI-R10	+00:49:36.637219	W LC_Init (73.80 kbps)	< 2100 (82.47 kbps)
147	HDCP	HDMI-R10	+00:49:36.659173	R RxStatus (73.69 kbps)	R Read_Message (73.80 kbps)
148	HDCP	HDMI-R10	+00:49:36.659337	< 2100 (82.47 kbps)	< LC_Send_L_prime (82.47 kbps)
149	HDCP	HDMI-R10	+00:49:36.660156	R Read_Message (73.80 kbps)	W SKE_Send_Eks (73.91 kbps)
150	HDCP	HDMI-R10	+00:49:36.660484	< LC_Send_L_prime (82.47 kbps)	R RxStatus (73.80 kbps)
151	HDCP	HDMI-R10	+00:49:36.672280	W SKE_Send_Eks (73.91 kbps)	< 0000 (82.47 kbps)
152	HDCP	HDMI-R10	+00:49:36.879371	R RxStatus (73.80 kbps)	R RxStatus (73.69 kbps)
153	HDCP	HDMI-R10	+00:49:36.879698	< 0000 (82.47 kbps)	< 0000 (82.47 kbps)
154	HDCP	HDMI-R10	+00:49:37.080563	R RxStatus (73.69 kbps)	< 0000 (82.47 kbps)
155	HDCP	HDMI-R10	+00:49:37.080727	< 0000 (82.47 kbps)	R RxStatus (73.80 kbps)
156	HDCP	HDMI-R10	+00:49:37.281592	R RxStatus (73.80 kbps)	

Type: EDID  
Start Time: +00:49:32.400217  
Duration: 14.090 msec  
Maximum I2C Rate: 82.61 kbps  
Read 128 bytes.

\* START \*

0000 A1 02 03 4D F0 52 10 05 | . . . M . R . .  
0008 20 22 04 03 02 07 06 5D | . . . . . ]  
0010 5E 5F 60 61 62 64 65 66 | ^ . . a b d e f  
0018 23 0F 7F 07 78 03 0C 00 | # . . . x . . .  
0020 10 00 F8 3C 2F C8 8A 01 | . . . < / . . .  
0028 02 03 04 81 41 00 16 06 | . . . . . A . . .  
0030 08 00 56 58 00 67 D8 5D | . . . V X . g . ]  
0038 C4 01 78 88 07 E2 00 4B | . . . x . . . K  
0040 83 7F 00 00 E1 0F E3 06 | . . . . .  
0048 0F 01 E3 05 FF 00 01 1D | . . . . .  
0050 80 18 71 1C 16 20 58 2C | . . . q . . . X  
0058 25 00 BA 88 21 00 00 9E | . . . ! . . . !  
0060 66 21 56 AA 51 00 1E 30 | . . . f | V . Q . . 0  
0068 46 8F 33 00 BA 88 21 00 | . . . F . 3 . . . !  
0070 00 1E 00 00 00 00 00 | . . . . .  
0078 00 00 00 00 00 00 00 | . . . . .  
0080 88-  
\* STOP \*

127: < 128 bytes (82.61 kbps)

# Aux Channel Analyzer (ACA) – HDCP Repeater Authentication

- ◆ HDMI Aux Channel Analyzer (ACA) for DDC monitoring:
  - ◆ Enables monitoring and analysis of the HDMI connection sequence.
  - ◆ Verify EDID exchange, HDCP authentication transactions.
  - ◆ Supports search and filtering functions.
  - ◆ Assigns precise timestamps for each transaction; provides user controls to associate events.
  - ◆ Enables export of transaction logs to share with colleagues.

The screenshot displays the ACA Data Viewer interface. The main window shows a list of events with columns for time, source, destination, and data. A yellow arrow points to the event at 00:14:51.762106, which is a RepeaterAuth\_Send\_ReceiverID\_List transaction. The right-hand pane provides a detailed view of this transaction, including the message type (HDCP), start time, duration, and a table of device capabilities.

ACA Data Viewer

Open Close Export Options Filter Find

[ACMT\_PT\_Rpt\_1\_Pass] Events: 73

Time	Source	Destination	Data
0	DPHP	DP-T60	+00:14:19.537922 WFD Falling Edge
1	HDCP	HDMI-R30	+00:14:50.714037 R HDCP2Version (73.91 kbps)
2	HDCP	HDMI-R30	+00:14:50.714365 < 04 (82.47 kbps)
3	HDCP	HDMI-R30	+00:14:50.719936 R RxStatus (73.80 kbps)
4	HDCP	HDMI-R30	+00:14:50.720263 < 0000 (82.47 kbps)
5	HDCP	HDMI-R30	+00:14:50.727308 W AKE_Init (73.91 kbps)
6	HDCP	HDMI-R30	+00:14:50.783013 R RxStatus (73.80 kbps)
7	HDCP	HDMI-R30	+00:14:50.783341 < 1602 (82.47 kbps)
8	HDCP	HDMI-R30	+00:14:50.784160 R Read_Message (73.91 kbps)
9	HDCP	HDMI-R30	+00:14:50.784488 < AKE_Send_Cert (82.61 kbps)
10	HDCP	HDMI-R30	+00:14:51.030080 W AKE_No_Stored_km (74.02 kbps)
11	HDCP	HDMI-R30	+00:14:51.246837 R RxStatus (73.91 kbps)
12	HDCP	HDMI-R30	+00:14:51.247165 < 0000 (82.47 kbps)
13	HDCP	HDMI-R30	+00:14:51.448029 R RxStatus (73.91 kbps)
14	HDCP	HDMI-R30	+00:14:51.448357 < 2100 (82.47 kbps)
15	HDCP	HDMI-R30	+00:14:51.449176 R Read_Message (73.91 kbps)
16	HDCP	HDMI-R30	+00:14:51.449340 < AKE_Send_R_prime (82.47 kbps)
17	HDCP	HDMI-R30	+00:14:51.503734 R RxStatus (73.80 kbps)
18	HDCP	HDMI-R30	+00:14:51.504062 < 1100 (82.47 kbps)
19	HDCP	HDMI-R30	+00:14:51.504881 R Read_Message (73.80 kbps)
20	HDCP	HDMI-R30	+00:14:51.505045 < AKE_Send_Pairing_Info (82.47 kbps)
21	HDCP	HDMI-R30	+00:14:51.518643 W LC_Init (73.91 kbps)
22	HDCP	HDMI-R30	+00:14:51.540598 R RxStatus (73.80 kbps)
23	HDCP	HDMI-R30	+00:14:51.540761 < 2100 (82.47 kbps)
24	HDCP	HDMI-R30	+00:14:51.541581 R Read_Message (73.91 kbps)
25	HDCP	HDMI-R30	+00:14:51.541908 < LC_Send_L_prime (82.47 kbps)
26	HDCP	HDMI-R30	+00:14:51.553705 W SKL_Send_Eks (73.91 kbps)
27	HDCP	HDMI-R30	+00:14:51.760795 R RxStatus (73.80 kbps)
28	HDCP	HDMI-R30	+00:14:51.761123 < 1B04 (82.47 kbps)
29	HDCP	HDMI-R30	+00:14:51.761942 R Read_Message (73.80 kbps)
30	HDCP	HDMI-R30	+00:14:51.762106 < RepeaterAuth_Send_ReceiverID_List (82.47 kbps)
31	HDCP	HDMI-R30	+00:14:51.769642 W RepeaterAuth_Send_Ack (73.91 kbps)
32	HDCP	HDMI-R30	+00:14:51.776851 W RepeaterAuth_Stream_Manage (73.91 kbps)
33	HDCP	HDMI-R30	+00:14:51.833211 R RxStatus (73.80 kbps)
34	HDCP	HDMI-R30	+00:14:51.833375 < 2100 (82.47 kbps)
35	HDCP	HDMI-R30	+00:14:51.834194 R Read_Message (73.91 kbps)
36	HDCP	HDMI-R30	+00:14:51.834522 < RepeaterAuth_Stream_Ready (82.47 kbps)

Type: HDCP  
Start Time: +00:14:51.762106  
Duration: 3.113 msec  
Maximum I2C Rate: 82.47 kbps  
Read: 27 bytes  
Register: 80h  
Name: Read\_Message  
Message: RepeaterAuth\_Send\_ReceiverID\_List (27 bytes)  
msg\_id: 12  
RxInfo:  
Bit Name Value Description  
0 HDCP1\_DEVICE\_DOWNSTREAM Y(1)  
1 HDCP2\_LEGACY\_DEVICE\_DOWNSTREAM N(0)  
2 MAX\_CASCADE\_EXCEEDED N(0)  
3 MAX\_DEVS\_EXCEEDED N(0)  
8-4 DEVICE\_COUNT 1  
11-9 DEPTH 1  
15-12 Rsvd 0  
seq\_num\_V: 0 (0000000h)  
V[255..128]: 02 F3 D5 D6 A0 1E 87 04 DC 51 26 80 CD 3C A0  
Receiver ID List:  
ID=00: 570CEBA925  
\* START \*  
0000 75 0C 02 11 00 00 00 02 | u . . . . .  
0008 F3 D5 D6 A0 1E 87 04 DC | . . . . .  
0010 51 26 80 CD 3C A0 BE 57 | Q & . . . . W  
0018 0C EB A9 25- | . . . . .  
\* STOP \*

30: < RepeaterAuth\_Send\_ReceiverID\_List (82.47 kbps)



# Aux Channel Analyzer (ACA) – Filtering

## ◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Filter the transaction list by interface, by type of transaction or by text strings.
- ◆ Search for specific transactions by text in the label text in the details of the message.

The screenshot displays the ACA Data Viewer application. The main window shows a list of transactions with columns for Open, Close, Export, Options, Filter, and Find. The transactions are filtered by Source (HDMI-R60) and Type (SCDC). The details pane on the right shows the selected transaction's details, including Type (SCDC), Start Time, Duration, Maximum I2C Rate, and Request Read from.

The ACA Filter dialog box is open, showing the filter criteria: `Where Src=HDMI-R60 AND Type=(EDID|SCDC|SCDC_...`. The dialog has tabs for Source, Type, Label, and Detail. The Text contains: field is set to `R Status`, and the Regular Expression Syntax checkbox is checked.

Open	Close	Export	Options	Filter	Find
0	SCDC	HDMI-R60	+00:35:51.358896	R Status_Flags_0	(48.86 kbps)
1	SCDC	HDMI-R60	+00:35:51.361681	R Status_Flags_0	(48.86 kbps)
2	SCDC	HDMI-R60	+00:35:51.364466	R Status_Flags_0	(48.86 kbps)
3	SCDC	HDMI-R60	+00:35:51.367252	R Status_Flags_0	(48.86 kbps)
4	SCDC	HDMI-R60	+00:35:51.370201	R Status_Flags_0	(48.86 kbps)
5	SCDC	HDMI-R60	+00:35:51.372986	R Status_Flags_0	(48.86 kbps)
6	SCDC	HDMI-R60	+00:35:51.375771	R Status_Flags_0	(48.86 kbps)
7	SCDC	HDMI-R60	+00:35:51.378556	R Status_Flags_0	(48.86 kbps)
8	SCDC	HDMI-R60	+00:35:51.381342	R Status_Flags_0	(48.86 kbps)
9	SCDC	HDMI-R60	+00:35:51.388223	R Status_Flags_0	(48.86 kbps)
10	SCDC	HDMI-R60	+00:35:51.391172	R Status_Flags_0	(48.86 kbps)
11	SCDC	HDMI-R60	+00:35:51.393957	R Status_Flags_0	(48.86 kbps)
12	SCDC	HDMI-R60	+00:35:51.396742	R Status_Flags_0	(48.86 kbps)
13	SCDC	HDMI-R60	+00:35:51.399528	R Status_Flags_0	(48.86 kbps)
14	SCDC	HDMI-R60	+00:35:51.402477	R Status_Flags_0	(48.86 kbps)
15	SCDC	HDMI-R60	+00:35:51.405262	R Status_Flags_0	(48.86 kbps)
16	SCDC	HDMI-R60	+00:35:51.408047	R Status_Flags_0	(48.86 kbps)
17	SCDC	HDMI-R60	+00:35:51.410832	R Status_Flags_0	(48.86 kbps)
18	SCDC	HDMI-R60	+00:35:51.413618	R Status_Flags_0	(48.86 kbps)
19	SCDC	HDMI-R60	+00:35:51.416403	R Status_Flags_0	(48.86 kbps)
20	SCDC	HDMI-R60	+00:35:51.419352	R Status_Flags_0	(48.86 kbps)
21	SCDC	HDMI-R60	+00:35:51.422137	R Status_Flags_0	(48.86 kbps)
22	SCDC	HDMI-R60	+00:35:51.424922	R Status_Flags_0	(48.86 kbps)
23	SCDC	HDMI-R60	+00:35:51.427708	R Status_Flags_0	(48.86 kbps)
24	SCDC	HDMI-R60	+00:35:51.430493	R Status_Flags_0	(48.86 kbps)
25	SCDC	HDMI-R60	+00:35:51.433442	R Status_Flags_0	(48.86 kbps)
26	SCDC	HDMI-R60	+00:35:51.436227	R Status_Flags_0	(48.86 kbps)
27	SCDC	HDMI-R60	+00:35:51.439668	R Status_Flags_0	(48.86 kbps)
28	SCDC	HDMI-R60	+00:35:51.442453	R Status_Flags_0	(48.86 kbps)
29	SCDC	HDMI-R60	+00:35:51.445402	R Status_Flags_0	(48.86 kbps)
30	SCDC	HDMI-R60	+00:35:51.448187	R Status_Flags_0	(48.86 kbps)
31	SCDC	HDMI-R60	+00:35:51.450973	R Status_Flags_0	(48.86 kbps)
32	SCDC	HDMI-R60	+00:35:51.453758	R Status_Flags_0	(48.86 kbps)
33	SCDC	HDMI-R60	+00:35:51.456543	R Status_Flags_0	(48.86 kbps)
34	SCDC	HDMI-R60	+00:35:51.459328	R Status_Flags_0	(48.86 kbps)

# Aux Channel Analyzer (ACA) – Filtering

## ◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Filter the transaction list by interface, by type of transaction or by text strings.
- ◆ Search for specific transactions by text in the label text in the details of the message.

ACA Data Viewer

Open Close Export Options Filter Find

[AA\_HDMI\_21\_12G\_10G\_FRL\_LT] Events: 866 (866)

0	SCDC	HDMI-R60	+00:35:51.354636	R Update_0 (48.86 kbps)
1	SCDC	HDMI-R60	+00:35:51.355128	< 00 (48.86 kbps)
2	SCDC	HDMI-R60	+00:35:51.355455	W Update_0 00 (48.86 kbps)
3	SCDC	HDMI-R60	+00:35:51.356111	R Update_0 (48.86 kbps)
4	SCDC	HDMI-R60	+00:35:51.356438	< 00 (48.86 kbps)
5	SCDC	HDMI-R60	+00:35:51.356930	W Update_0 00 (48.86 kbps)
6	SCDC	HDMI-R60	+00:35:51.357421	R Sink Version (48.86 kbps)
7	SCDC	HDMI-R60	+00:35:51.357913	< 01 (48.86 kbps)
8	SCDC	HDMI-R60	+00:35:51.358241	W Source Version 01 (48.86 kbps)
9	SCDC	HDMI-R60	+00:35:51.358811	R Status_Flags_0 (48.86 kbps)
10	SCDC	HDMI-R60	+00:35:51.361811	< 01 (48.86 kbps)
11	SCDC	HDMI-R60	+00:35:51.362173	R Status_Flags_0 (48.86 kbps)
12	SCDC	HDMI-R60	+00:35:51.364466	< 01 (48.86 kbps)
13	SCDC	HDMI-R60	+00:35:51.364958	R Status_Flags_0 (48.86 kbps)
14	SCDC	HDMI-R60	+00:35:51.367252	< 01 (48.86 kbps)
15	SCDC	HDMI-R60	+00:35:51.367743	R Status_Flags_0 (48.86 kbps)
16	SCDC	HDMI-R60	+00:35:51.370201	< 01 (48.86 kbps)
17	SCDC	HDMI-R60	+00:35:51.370528	R Status_Flags_0 (48.86 kbps)
18	SCDC	HDMI-R60	+00:35:51.372986	< 01 (48.86 kbps)
19	SCDC	HDMI-R60	+00:35:51.373314	R Status_Flags_0 (48.86 kbps)
20	SCDC	HDMI-R60	+00:35:51.373771	< 01 (48.86 kbps)
21	SCDC	HDMI-R60	+00:35:51.376099	R Status_Flags_0 (48.86 kbps)
22	SCDC	HDMI-R60	+00:35:51.378556	< 01 (48.86 kbps)
23	SCDC	HDMI-R60	+00:35:51.378884	R Status_Flags_0 (48.86 kbps)
24	SCDC	HDMI-R60	+00:35:51.381342	< 01 (48.86 kbps)
25	SCDC	HDMI-R60	+00:35:51.381669	R Status_Flags_0 (48.86 kbps)
26	SCDC	HDMI-R60	+00:35:51.382223	< 01 (48.86 kbps)
27	SCDC	HDMI-R60	+00:35:51.388714	R Status_Flags_0 (48.86 kbps)
28	SCDC	HDMI-R60	+00:35:51.391172	< 01 (48.86 kbps)
29	SCDC	HDMI-R60	+00:35:51.391500	R Status_Flags_0 (48.86 kbps)
30	SCDC	HDMI-R60	+00:35:51.393957	< 01 (48.86 kbps)
31	SCDC	HDMI-R60	+00:35:51.394285	R Status_Flags_0 (48.86 kbps)
32	SCDC	HDMI-R60	+00:35:51.396742	< 01 (48.86 kbps)
33	SCDC	HDMI-R60	+00:35:51.397234	R Status_Flags_0 (48.86 kbps)
34	SCDC	HDMI-R60	+00:35:51.397234	< 01 (48.86 kbps)

Type: SCDC  
Start Time: +00:35:51.359224  
Duration: 328 to 492 us  
Maximum I2C Rate: 48.86 kbps  
Read, 1 byte  
40h: Status\_Flags\_0

Bit	Name	Value	Description
0	Clock_Detected	Y (1)	
1	Ch0_In0_Locked	N (0)	
2	Ch1_In1_Locked	N (0)	
3	Ch2_In2_Locked	N (0)	
4	Lane3_Locked	N (0)	
5		0	Reserved
6	FLT_ready	N (0)	
7	DSC_DecoderFail	N (0)	

ACA Filter

Open Save Clear Add Remove

Where Type=(EDID|SCDC|SCDC\_UP|HDCP|HDMI-HFD)

Source	Type	Label	Detail
<input type="checkbox"/> NOT			
Other			
<input type="checkbox"/> Other DDC			
<input checked="" type="checkbox"/> HDCP			
<input checked="" type="checkbox"/> EDID			
<input type="checkbox"/> CEC			
<input checked="" type="checkbox"/> SCDC			
<input type="checkbox"/> I2C-SDA-FE			
<input type="checkbox"/> I2C-SDA-RE			
<input type="checkbox"/> I2C-SCL-FE			
<input type="checkbox"/> I2C-SCL-RE			
<input checked="" type="checkbox"/> HDMI-HPD			
<input checked="" type="checkbox"/> SCDC_UP			
<input type="checkbox"/> IDCC			

OK CANCEL

# Aux Channel Analyzer (ACA) – Searching

## ◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Filter the transaction list by interface, by type of transaction or by text strings.
- ◆ Search for specific transactions by text in the label text in the details of the message.

The screenshot displays the ACA Data Viewer application. The main window shows a list of transactions with columns for Open, Close, Export, Options, Filter, and Find. The transactions are filtered by 'Type: SCDC' and 'Interface: HDMI-R60'. A yellow arrow points to the 'Find' column header. Another yellow arrow points to the 'Status\_Flags\_0' field in the transaction details pane.

The transaction list shows the following data:

Open	Close	Export	Options	Filter	Find
0	SCDC	HDMI-R60	+00:35:51.354636	R Update_0 (48.86 kbps)	
1	SCDC	HDMI-R60	+00:35:51.355128	< 00 (48.86 kbps)	
2	SCDC	HDMI-R60	+00:35:51.355455	W Update_0 00 (48.86 kbps)	
3	SCDC	HDMI-R60	+00:35:51.356111	R Update_0 (48.86 kbps)	
4	SCDC	HDMI-R60	+00:35:51.356438	< 00 (48.86 kbps)	
5	SCDC	HDMI-R60	+00:35:51.356930	W Update_0 00 (48.86 kbps)	
6	SCDC	HDMI-R60	+00:35:51.357421	R Sink Version (48.86 kbps)	
7	SCDC	HDMI-R60	+00:35:51.357913	< 01 (48.86 kbps)	
8	SCDC	HDMI-R60	+00:35:51.358241	W Source Version 01 (48.86 kbps)	
9	SCDC	HDMI-R60	+00:35:51.358896	R Status_Flags_0 (48.86 kbps)	
10	SCDC	HDMI-R60	+00:35:51.359224	< 01 (48.86 kbps)	
11	SCDC	HDMI-R60	+00:35:51.361668	R Status_Flags_0 (48.86 kbps)	
12	SCDC	HDMI-R60	+00:35:51.364446	< 01 (48.86 kbps)	
13	SCDC	HDMI-R60	+00:35:51.364958	R Status_Flags_0 (48.86 kbps)	
14	SCDC	HDMI-R60	+00:35:51.367252	R Status_Flags_0 (48.86 kbps)	
15	SCDC	HDMI-R60	+00:35:51.367743	< 01 (48.86 kbps)	
16	SCDC	HDMI-R60	+00:35:51.370201	R Status_Flags_0 (48.86 kbps)	
17	SCDC	HDMI-R60	+00:35:51.370528	< 01 (48.86 kbps)	
18	SCDC	HDMI-R60	+00:35:51.372986	R Status_Flags_0 (48.86 kbps)	
19	SCDC	HDMI-R60	+00:35:51.373314	< 01 (48.86 kbps)	
20	SCDC	HDMI-R60	+00:35:51.375771	R Status_Flags_0 (48.86 kbps)	
21	SCDC	HDMI-R60	+00:35:51.376099	< 01 (48.86 kbps)	
22	SCDC	HDMI-R60	+00:35:51.378556	R Status_Flags_0 (48.86 kbps)	
23	SCDC	HDMI-R60	+00:35:51.378884	< 01 (48.86 kbps)	
24	SCDC	HDMI-R60	+00:35:51.381342	R Status_Flags_0 (48.86 kbps)	
25	SCDC	HDMI-R60	+00:35:51.381669	< 01 (48.86 kbps)	
26	SCDC	HDMI-R60	+00:35:51.388223	R Status_Flags_0 (48.86 kbps)	
27	SCDC	HDMI-R60	+00:35:51.388714	< 01 (48.86 kbps)	
28	SCDC	HDMI-R60	+00:35:51.391172	R Status_Flags_0 (48.86 kbps)	
29	SCDC	HDMI-R60	+00:35:51.391500	< 01 (48.86 kbps)	
30	SCDC	HDMI-R60	+00:35:51.393957	R Status_Flags_0 (48.86 kbps)	
31	SCDC	HDMI-R60	+00:35:51.394285	< 01 (48.86 kbps)	
32	SCDC	HDMI-R60	+00:35:51.396742	R Status_Flags_0 (48.86 kbps)	
33	SCDC	HDMI-R60	+00:35:51.397234	< 01 (48.86 kbps)	
34	SCDC	HDMI-R60	+00:35:51.397234	< 01 (48.86 kbps)	

The transaction details pane shows the following information:

- Type: SCDC
- Start Time: +00:35:51.362173
- Duration: 164 to 328 us
- Maximum I2C Rate: 48.86 kbps
- Read, 1 byte
- 40h: Status\_Flags\_0

The bit field table shows the following data:

Bit	Name	Value	Description
0	Ch0_Detected	Y(1)	
1	Ch0_Locked	N(0)	
2	Ch1_Locked	N(0)	
3	Ch2_Locked	N(0)	
4	Ch3_Locked	N(0)	

The ACA Find dialog box is open, showing the search criteria: 'Where Src=HDMI-R60 AND Type=(EDID|SCDC|SCDC\_UP|HDCP) AND ...'. The 'Text contains' field is empty, and the 'Regular Expression Syntax' checkbox is checked. The 'Found Event #13' button is visible.

# Aux Channel Analyzer (ACA) – Export Transaction Data

## ◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Save ACA log as an HTML file.
- ◆ Export capture data to disseminate to colleagues, other subject matter experts or Teledyne Customer Support.
- ◆ Exported capture does not require 980 48G module instrument; only requires ATP Manager.
- ◆ Transfer to PC to save and recall later for analysis.

The screenshot displays the ACA Data Viewer application. The main window shows a list of events with columns for time, source, destination, and data. A yellow arrow points to the 'Export' button in the top menu. Another yellow arrow points to the 'Export as...' button in the 'Events' dialog box. The dialog box is open, showing options for 'Events' (All, Range) and 'File Format' (Text, HTML). The 'Range' option is selected for events, and the 'HTML' format is chosen. The 'Show Time Delta' checkbox is checked, and 'Show Details' and 'Show Raw Data' are also checked. The 'OK' button is highlighted.

Time	Source	Destination	Data
0	SCDC	HDMI-R60	+00:35:51.354636 R Update_0 (48.86 kbps)
1	SCDC	HDMI-R60	+00:35:51.355128 < 00 (48.86 kbps)
2	SCDC	HDMI-R60	+00:35:51.355455 W Update_0 00 (48.86 kbps)
3	SCDC	HDMI-R60	+00:35:51.356111 R Update_0 (48.86 kbps)
4	SCDC	HDMI-R60	+00:35:51.356438 < 00 (48.86 kbps)
5	SCDC	HDMI-R60	+00:35:51.356930 W Update_0 00 (48.86 kbps)
6	SCDC	HDMI-R60	+00:35:51.357421 R Sink Version (48.86 kbps)
7	SCDC	HDMI-R60	+00:35:51.357913 < 01 (48.86 kbps)
8	SCDC	HDMI-R60	+00:35:51.358241 W Source Version 01 (48.86 kbps)
9	SCDC	HDMI-R60	+00:35:51.358896 R Status_Flags_0 (48.86 kbps)
10	SCDC	HDMI-R60	+00:35:51.359224 < 01 (48.86 kbps)
11	SCDC	HDMI-R60	+00:35:51.361681 R Status_Flags_0 (48.86 kbps)
12	SCDC	HDMI-R60	+00:35:51.362173 < 01 (48.86 kbps)
13	SCDC	HDMI-R60	+00:35:51.364466 R Status_Flags_0 (48.86 kbps)
14	SCDC	HDMI-R60	+00:35:51.364958 < 01 (48.86 kbps)
15	SCDC	HDMI-R60	+00:35:51.367252 R Status_Flags_0 (48.86 kbps)
16	SCDC	HDMI-R60	+00:35:51.367743 < 01 (48.86 kbps)
17	SCDC	HDMI-R60	+00:35:51.370201 R Status_Flags_0 (48.86 kbps)
18	SCDC	HDMI-R60	+00:35:51.370528 < 01 (48.86 kbps)
19	SCDC	HDMI-R60	+00:35:51.372986 R Status_Flags_0 (48.86 kbps)
20	SCDC	HDMI-R60	+00:35:51.373314 < 01 (48.86 kbps)
21	SCDC	HDMI-R60	+00:35:51.375771 R Status_Flags_0 (48.86 kbps)
22	SCDC	HDMI-R60	+00:35:51.376099 < 01 (48.86 kbps)
23	SCDC	HDMI-R60	+00:35:51.378556 R Status_Flags_0 (48.86 kbps)
24	SCDC	HDMI-R60	+00:35:51.378884 < 01 (48.86 kbps)
25	SCDC	HDMI-R60	+00:35:51.381342 R Status_Flags_0 (48.86 kbps)
26	SCDC	HDMI-R60	+00:35:51.381669 < 01 (48.86 kbps)
27	SCDC	HDMI-R60	+00:35:51.388223 R Status_Flags_0 (48.86 kbps)
28	SCDC	HDMI-R60	+00:35:51.388714 < 01 (48.86 kbps)
29	SCDC	HDMI-R60	+00:35:51.391172 R Status_Flags_0 (48.86 kbps)
30	SCDC	HDMI-R60	+00:35:51.391500 < 01 (48.86 kbps)
31	SCDC	HDMI-R60	+00:35:51.393957 R Status_Flags_0 (48.86 kbps)
32	SCDC	HDMI-R60	+00:35:51.394285 < 01 (48.86 kbps)
33	SCDC	HDMI-R60	+00:35:51.396742 R Status_Flags_0 (48.86 kbps)
34	SCDC	HDMI-R60	+00:35:51.397234 < 01 (48.86 kbps)

ACA Data Viewer

Export Options Filter Find

12G\_10G\_FRL\_LT Events: 866 (866)

Type: SCDC  
Start Time: +00:35:51.364958  
Duration: 328 to 492 us  
Maximum I2C Rate: 48.86 kbps

Read, 1 byte  
40h: Status\_Flags\_0

Bit	Name	Value	Description
0	Clock_Detected	Y(1)	
1	Ch0_Ln0_Locked	N(0)	
2	Ch1_Ln1_Locked	N(0)	
3	Ch2_Ln2_Locked	N(0)	
4	Lane3_Locked	N(0)	
5		0	Reserved
6	FLT		
7	DSC		

Export as...

\* START \*  
0000 A9 01-  
\* STOP \*

Events  
All Range  
Max Range: 1 - 866  
Start: 1  
End: 1

Show Time Delta ☒

Show Details ☒

Show Raw Data ☒

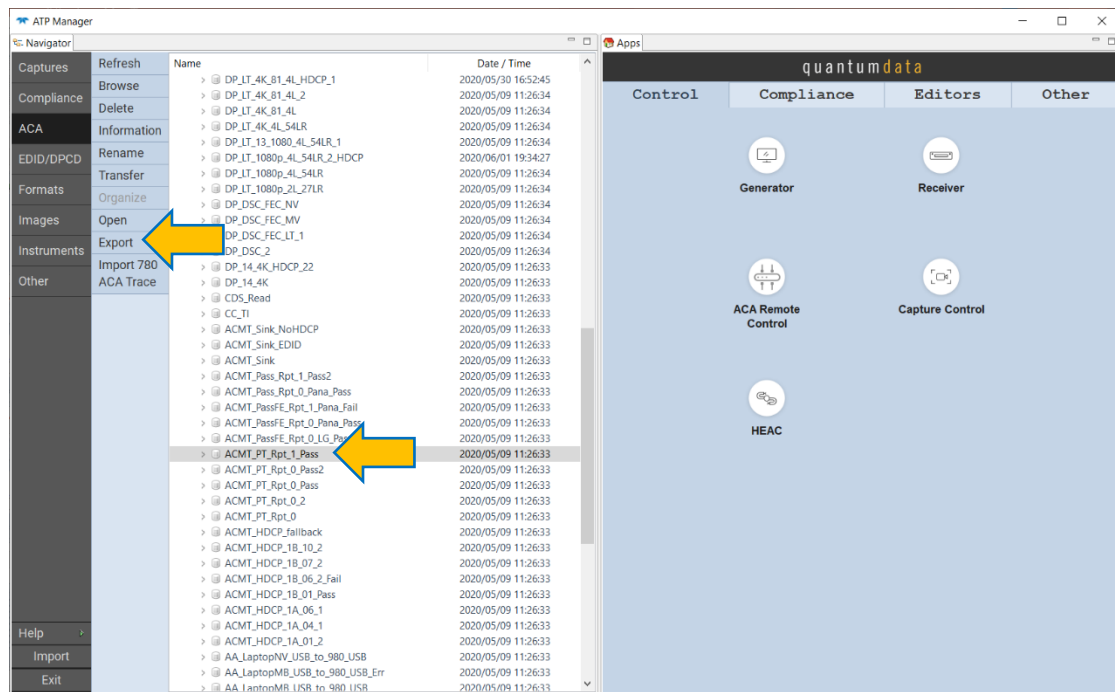
File Format  
Text HTML

OK CANCEL

# Aux Channel Analyzer (ACA) – Export Transaction Data

## ◆ HDMI Aux Channel Analyzer (ACA) Export:

- ◆ Save ACA log as an HTML file.
- ◆ Export capture data to disseminate to colleagues, other subject matter experts or Teledyne Customer Support.
- ◆ Exported capture does not require 980 48G module instrument; only requires ATP Manager.
- ◆ Transfer to PC to save and recall later for analysis.



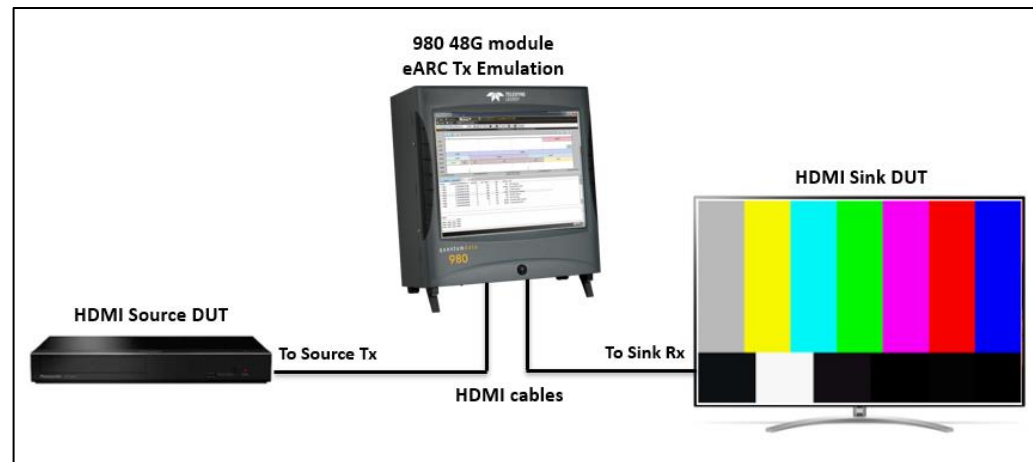


# HDMI DDC Passive Monitoring TMDS and FRL modes



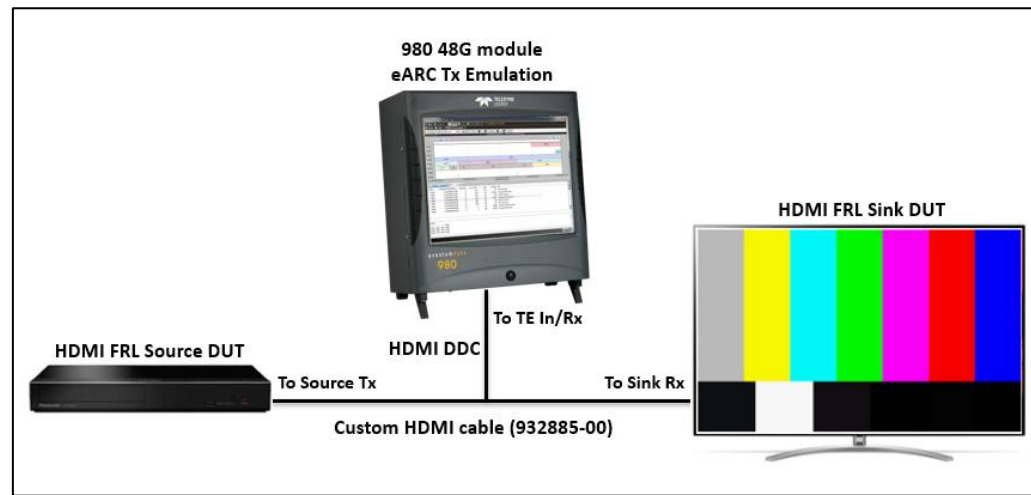
# HDMI DDC Passive Monitoring – TMDS Mode

- ◆ Passive monitoring of DDC channel
  - ◆ You can monitor the DDC channel passively in the **TMDS** mode by connecting a source to the 980 48G module Rx port and a sink to the 980 48G module Tx port.
  - ◆ The ability to passively monitor the DDC channel in the TMDS mode is important for EDID and HDCP authentication interoperability.



# HDMI DDC Passive Monitoring – FRL Mode

- ◆ Passive monitoring of DDC channel
  - ◆ You can optionally monitor the DDC channel passively in the **FRL** mode using a custom cable (setup right).
  - ◆ The DDC passive monitoring enables you to diagnose interoperability problems between a source and a display.
  - ◆ The ability to passively monitor the DDC channel in the FRL mode with the custom cable is especially important for FRL link training, EDID and HDCP authentication interoperability.



# HDMI 2.1 Source Testing Compliance Testing



# HDMI Fixed Rate Link (FRL) Source Compliance Test

## ◆ HDMI 2.1 FRL source compliance Testing:

- ◆ Run FRL source compliance tests. Full list of tests supported (only partial list shown right).



FRL Source			
Instrument: AL_M41d [10.30.196.30]		Connect	Cards
CDF Entry		Test Selection	Test Options / Preview
Select All	✓ ✗	Duration	Options
<b>Protocol</b>			
>	HFR1-11: Source FRL Protocol - Legal Codes		✓
>	HFR1-19: Source FRL Packets - FRL Map Characters		✓
>	HFR1-20: Source FRL Packets - FRL Control Periods		✓
>	HFR1-21: Source FRL Packets - Active Video FRL Packets (Uncompressed)		✓
>	HFR1-23: Source FRL Protocol - Data Flow Metering Variations		✓
<b>Link Training</b>			
>	HFR1-10: Source FRL Protocol - FRL Link Training Patterns		✓
>	HFR1-12: Source FRL Protocol - Successful FRL Link Training		✓
>	HFR1-13: Source FRL Protocol - FRL Link Training - Link Rate Change		✓
>	HFR1-17: Source FRL Protocol - FRL Link Training - Future Rate Support		✓
<b>8bpc Encoding</b>			
>	HFR1-29: Source Pixel Encoding (FRL Mode) - RGB		✓
>	HFR1-30: Source Pixel Encoding (FRL Mode) - YCBCR 4:2:2/4:4		✓
>	HFR1-31: Source Pixel Encoding (FRL Mode) - YCBCR 4:2:0		✓
<b>DC Encoding</b>			
>	HFR1-27: Source Pixel Encoding (FRL Mode) - Non-YCBCR 4:2:0 Deep Color		✓
>	HFR1-32: Source Pixel Encoding (FRL Mode) - YCBCR 4:2:0 Deep Color		✓
<b>8bpc Timing</b>			
>	HFR1-14: Source Video Timing (FRL Mode) - Sub-2160p 24-bit Color Depth		✓
>	HFR1-24: Source Video Timing (FRL Mode) - 2160p 24-bit Color Depth		✓
>	HFR1-33: Source Video Timing (FRL Mode) - YCBCR 4:2:0		✓
>	HFR1-50: Source Video Timing (FRL Mode) - 4320p 24-bit Color Depth		✓
<b>DC Timing</b>			
>	HFR1-15: Source Video Timing (FRL Mode) - Sub-2160p Deep Color		✓
>	HFR1-25: Source Video Timing (FRL Mode) - 2160p Deep Color		✓
>	HFR1-34: Source Video Timing (FRL Mode) - YCBCR 4:2:0 Deep Color		✓





# HDMI Fixed Rate Link (FRL) Source Compliance Test

- ◆ HDMI 2.1 FRL source compliance Testing:
  - ◆ Run FRL source compliance tests. Full list of tests supported.
  - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
  - ◆ Enables compliance self-testing and/or pre-testing of FRL devices.
  - ◆ Enables export of compliance test results to share with colleagues.

Compliance Test Results Viewer

FRL Source (2.1b) Compliance Test Results

Results Name: FW\_05\_14\_2019\_13\_28\_21  
Date Tested: May14, 2019 1:28 PM  
Overall Status: **CTS 2.1b - Incomplete**  
Manufacturer: Futurewei/Hisilicon  
Model Name: HiFoneV501  
Port Tested: 1  
HTML Report

Test Name / Details	Status
HFR1-11: Source FRL Protocol - Legal Codes	Pass
Iter 01: FRL 3 Lane Mode	Pass
Trained at: (2) 6 Gbps @ 3 Lanes	
01: Test that the FRL characters count and SSB/SR characters count is valid.	Pass
02: SR header occurs only after 32 super blocks and at SB count '0'.	Pass
03: Illegal codes or other related errors associated with this test case.	Pass
04: SSB/SR header occurs only prior to Character block '0'.	Pass
Iter 02: FRL 4 Lane Mode	Pass
HFR1-19: Source FRL Packets - FRL Map Characters	Pass
Iter 01: Lowest FRL Rate in 3 Lane mode	Pass
Iter 02: Lowest FRL Rate in 4 Lane mode	Pass
Trained at: (3) 6 Gbps @ 4 Lanes	
01: Test that the FRL MAP Type is valid.	Pass
02: Test that Video Blanking/Video Data Characters Length is greater than 1	Pass
03: Test That the sum of all MAP Length fields in a Super Block is 2008.	Pass
HFR1-20: Source FRL Packets - FRL Control Periods	Pass
HFR1-21: Source FRL Packets - Active Video FRL Packets (Uncompressed)	Fail
Iter 01: Lowest FRL Rate in 3 Lane mode	Fail
Trained at: (1) 3 Gbps @ 3 Lanes	
01: Test that the Source only outputs legal Active Video FRL Packets.	Fail
02: Test that the video data characters are not separated by video blanking	Pass
03: Test that the last second byte of the 16-bit value of active video data	Pass
Iter 02: Lowest FRL Rate in 4 Lane mode	Fail
HFR1-23: Source FRL Protocol - Data Flow Metering Variations	Pass
HFR1-12: Source FRL Protocol - Successful FRL Link Training	Pass
HFR1-13: Source FRL Protocol - FRL Link Training - Link Rate Change	Pass
HFR1-17: Source FRL Protocol - FRL Link Training - Future Rate Support	Pass

Open Capture

Instrument: SS980B [10.30.196.240]

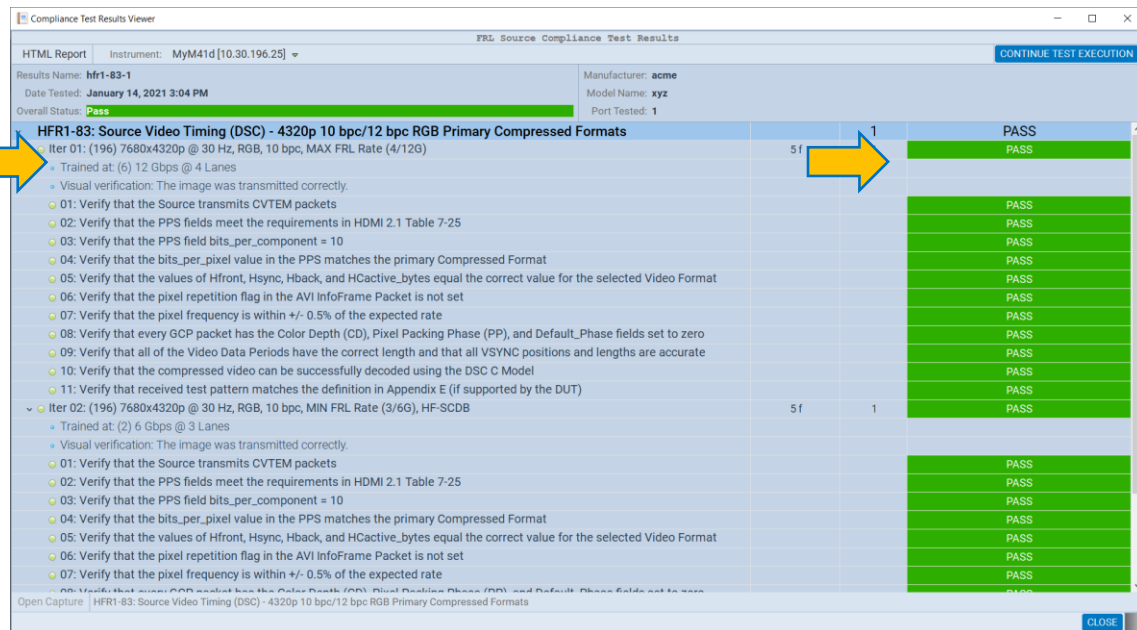
Continue Test Execution

Close

# HDMI FRL Display Stream Compression Source Compliance Test

## ◆ HDMI 2.1 FRL source compliance Testing:

- ◆ Run FRL DSC source compliance tests. Full list of tests supported.
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of FRL DSC devices.
- ◆ Enables export of compliance test results to share with colleagues.



FRL Source Compliance Test Results		
HTML Report	Instrument: MyM41d [10.30.196.25]	
Results Name: HFR1-83-1	Manufacturer: acme	
Date Tested: January 14, 2021 3:04 PM	Model Name: xyz	
Overall Status: <b>Pass</b>	Port Tested: 1	
<b>HFR1-83: Source Video Timing (DSC) - 4320p 10 bpc/12 bpc RGB Primary Compressed Formats</b>		
Iter 01: (196) 7680x4320p @ 30 Hz, RGB, 10 bpc, MAX FRL Rate (4/12G)	5 f	1
Trained at: (6) 12 Gbps @ 4 Lanes		<b>PASS</b>
Visual verification: The image was transmitted correctly.		<b>PASS</b>
01: Verify that the Source transmits CVTEM packets		<b>PASS</b>
02: Verify that the PPS fields meet the requirements in HDMI 2.1 Table 7-25		<b>PASS</b>
03: Verify that the PPS field bits_per_component = 10		<b>PASS</b>
04: Verify that the bits_per_pixel value in the PPS matches the primary Compressed Format		<b>PASS</b>
05: Verify that the values of Hfront, Hsync, Hback, and HActive_bytes equal the correct value for the selected Video Format		<b>PASS</b>
06: Verify that the pixel repetition flag in the AVI InfoFrame Packet is not set		<b>PASS</b>
07: Verify that the pixel frequency is within +/- 0.5% of the expected rate		<b>PASS</b>
08: Verify that every GCP packet has the Color Depth (CD), Pixel Packing Phase (PP), and Default_Phase fields set to zero		<b>PASS</b>
09: Verify that all of the Video Data Periods have the correct length and that all VSYNC positions and lengths are accurate		<b>PASS</b>
10: Verify that the compressed video can be successfully decoded using the DSC C Model		<b>PASS</b>
11: Verify that received test pattern matches the definition in Appendix E (if supported by the DUT)		<b>PASS</b>
Iter 02: (196) 7680x4320p @ 30 Hz, RGB, 10 bpc, MIN FRL Rate (3/6G), HF-SCDB	5 f	1
Trained at: (2) 6 Gbps @ 3 Lanes		<b>PASS</b>
Visual verification: The image was transmitted correctly.		<b>PASS</b>
01: Verify that the Source transmits CVTEM packets		<b>PASS</b>
02: Verify that the PPS fields meet the requirements in HDMI 2.1 Table 7-25		<b>PASS</b>
03: Verify that the PPS field bits_per_component = 10		<b>PASS</b>
04: Verify that the bits_per_pixel value in the PPS matches the primary Compressed Format		<b>PASS</b>
05: Verify that the values of Hfront, Hsync, Hback, and HActive_bytes equal the correct value for the selected Video Format		<b>PASS</b>
06: Verify that the pixel repetition flag in the AVI InfoFrame Packet is not set		<b>PASS</b>
07: Verify that the pixel frequency is within +/- 0.5% of the expected rate		<b>PASS</b>
08: Verify that every GCP packet has the Color Depth (CD), Pixel Packing Phase (PP), and Default_Phase fields set to zero		<b>PASS</b>
09: Verify that all of the Video Data Periods have the correct length and that all VSYNC positions and lengths are accurate		<b>PASS</b>
10: Verify that the compressed video can be successfully decoded using the DSC C Model		<b>PASS</b>
11: Verify that received test pattern matches the definition in Appendix E (if supported by the DUT)		<b>PASS</b>

# HDMI TMDS Source Compliance Testing

## ◆ HDMI TMDS compliance Testing:

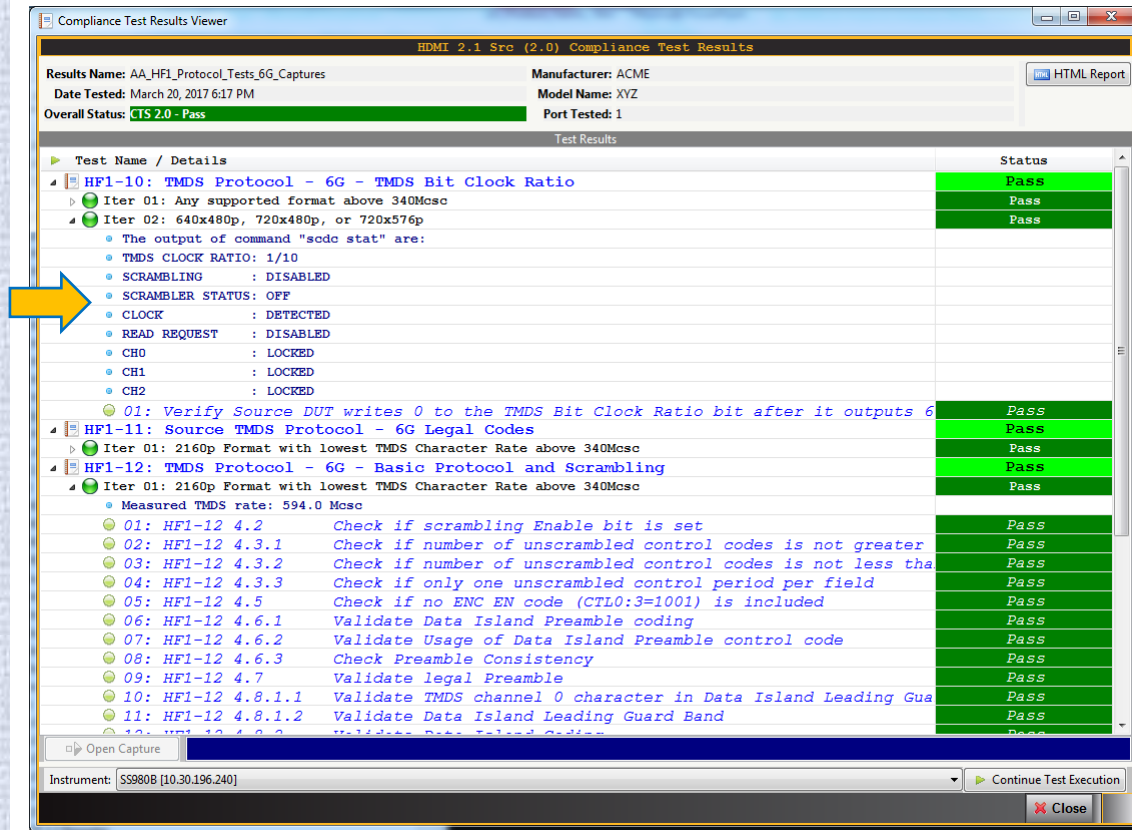
- ◆ Run TMDS source compliance tests. Full list of tests supported (only partial list shown right).
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of HDMI TMDS devices.
- ◆ Enables export of compliance test results to share with colleagues.

HDMI TMDS Source	
Instrument: AL_M41d [10.30.196.30]	Connect Cards
CDF Entry	Test Selection
Select All	Duration Options
<b>EXECUTE TESTS</b>	
<b>TMDS Protocol</b>	
> HF1-10: TMDS Protocol - 6G - TMDS Bit Clock Ratio	✓
> HF1-11: Source TMDS Protocol - 6G Legal Codes	✓
> HF1-12: TMDS Protocol - 6G - Basic Protocol and Scrambling	✓
> HF1-13: TMDS Protocol - Scrambling <= 3.4Gbps	✓
> HF1-21: TMDS Protocol - 6G - Legal Codes - other Video Timings	✓
> HF1-22: TMDS Protocol - 6G - Basic Protocol and Scrambling - Other Video Timings	✓
<b>Pixel Encoding</b>	
> HF1-31: Pixel Encoding - YCBCR 4:2:0 - TMDS Pixel Encoding	✓
> HF1-32: Pixel Encoding - YCBCR 4:2:0 Deep Color - TMDS Pixel Encoding	✓
<b>Video Timing</b>	
HF1-14: Video Timing - 6G - 2160p 24-bit Color Depth	✗
> HF1-15: Video Timing - 6G - Deep Color	✓
> HF1-16: Video Timing - 6G - 2160p 3D	✓
> HF1-24: Video Timing - 6G - Other 24-bit Color Depth	✓
> HF1-25: Video Timing - 6G - Other Deep Color	✓
> HF1-26: Video Timing - 6G - Non-2160p 3D	✓
> HF1-33: Video Timing - YCBCR 4:2:0	✓
> HF1-34: Video Timing - YCBCR 4:2:0 Deep Color	✓
> HF1-35: Video Timing - 21:9 (64:27)	✓
> HF1-71: Video Timing - YCbCr 4:2:0 for 861G Video Formats	✓
> HF1-72: Video Timing - YCbCr 4:2:0 Deep Color for 861G Video Formats	✓
<b>AVI-IF/GCP</b>	
> HF1-18: AVI InfoFrame - 6G	✓
> HF1-28: AVI InfoFrame - 6G - Other Video Timings	✓
> HF1-51: AVI InfoFrame for Y420VDB and Y420CMDB	✓
> HF1-52: AVI InfoFrame and GCP - YCbCr 4:2:0 BT.2020	✓

**CLOSE**

# HDMI TMDS Source Compliance Testing

- ◆ HDMI TMDS compliance Testing:
  - ◆ Run TMDS source compliance tests. Full list of tests supported.
  - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
  - ◆ Enables compliance self-testing and/or pre-testing of HDMI TMDS devices.
  - ◆ Enables export of compliance test results to share with colleagues.



# HDMI TMDS Gaming Source Compliance Test

- ◆ HDMI 2.1 TMDS Gaming sink compliance Testing:

- ◆ Run TMDS Gaming sink compliance tests:
  - ◆ Quick Frame Transport (QFT).
  - ◆ Variable Refresh Rate (VRR).
  - ◆ Quick Media Switching (QMS).
  - ◆ VRR with QFT.
  - ◆ ALLM – (Future)
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of TMDS Gaming-capable devices.
- ◆ Enables export of compliance test results to share w/ colleagues.

The screenshot shows the FRL Source application window. At the top, it displays "Instrument: MyM41h [10.30.196.32]" with expandable sections for "Connect" and "Cards". Below this is a header bar with three tabs: "CDF Entry", "Test Selection", and "Test Options / Preview". The main area has a toolbar with "Select All", a checkmark icon, a cross icon, "Duration", and "Options". A prominent green button labeled "EXECUTE TESTS" is on the right. The test results are listed under a collapsed "Gaming" category:

Test Name	Status	Result
<b>HF1-56: Auto Low-Latency Mode for Sources</b>		✓
• Iter 01: Source_Supports_ALLM = 'N': Automatic PASS(SKIP)	--	✓
<b>HF1-57: Quick Frame Transport for Sources</b>		✓
• Iter 01: Source_Supports_FVA = 'N': Automatic PASS(SKIP)	--	✓
<b>HF1-58: Variable Refresh Rate for Sources</b>		✓
• Iter 01: Source_Supports_VRR = 'N': Automatic PASS(SKIP)	--	✓
<b>HF1-59: Quick Media Switching for Sources</b>		✓
• Iter 01: Source_Supports_QMS = 'N': Automatic PASS(SKIP)	--	✓
<b>HF1-60: VRR with QFT for Sources</b>		✓
• Iter 01: Source_Supports_VRR = 'N': Automatic PASS(SKIP)	--	✓

A "CLOSE" button is located at the bottom right corner.



# HDMI TMDS Gaming Source Compliance Test

## ◆ HDMI 2.1 TMDS Gaming sink compliance Testing:

- ◆ Run TMDS Gaming sink compliance tests:
  - ◆ Quick Frame Transport (QFT).
  - ◆ Variable Refresh Rate (VRR).
  - ◆ Quick Media Switching (QMS).
  - ◆ VRR with QFT.
  - ◆ ALLM – (Future)
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of TMDS Gaming-capable devices.
- ◆ Enables export of compliance test results to share w/ colleagues.

The screenshot displays the FRL Source Compliance Test (2.1b) software interface. The main window is titled "FRL Source Compliance Test (2.1b): 'NK\_Game\_Matt'". It features a "Test List" window and a "Test Log" window.

**Test List Window:**

Category / Test Name	Status
<b>Gaming</b>	
HF1-56: Auto Low-Latency Mode for Sources	In Progress
Iter 01: Verify HF-VSIF with non-ALLM EDID	Fail
Iter 02: Verify HF-VSIF with ALLM EDID	Pass
Iter 03: Verify Video	In Progress
HF1-57: Quick Frame Transport for Sources	Incomplete
Iter 01: 720p60 RGB 8 bpc, FF1: No VTEMs Transmitted	Not Tested
Iter 02: Timing #1: 1920x1080-60 FF2-4	Not Tested
Iter 03: Interlaced	User Skipped
Iter 04: Any Timing, FVA Factor=2	User Skipped
Iter 05: Any Timing, Highest Supported FVA Factor	User Skipped
HF1-58: Variable Refresh Rate for Sources	Incomplete
Iter 01: VRR48-60, VRR Disabled	Not Tested
Iter 02: 1080p60 RGB 8 bpc, VRR48-60	Not Tested
Iter 03: 1080p60 RGB 8 bpc, VRR48-60, Stressed	User Skipped
Iter 04: 1080p120 RGB 8 bpc, VRR48-60	User Skipped
Iter 05: 1080p120 RGB 8 bpc, VRR48-60, Stressed	User Skipped
Iter 06: 1080p120 RGB 8 bpc, VRR48-100	User Skipped
Iter 07: 1080p120 RGB 8 bpc, VRR48-100, Stressed	User Skipped
Iter 08: 1080p120 RGB 8 bpc, VRR48-110	User Skipped
Iter 09: 1080p120 RGB 8 bpc, VRR48-110, Stressed	User Skipped
Iter 10: 1080p120 RGB 8 bpc, VRR48-120	User Skipped
Iter 11: 1080p120 RGB 8 bpc, VRR48-120, Stressed	User Skipped

**Test Log Window:**

Line	Message
0103	Capturing data...
0104	Post Capture Processing
0105	Generating video content data...
0106	-- preprocess 0 frames
0107	-- preprocess 14 frames
0150	-- preprocess 440 frames
0151	Preparing verification images
0152	Generating a verification image.

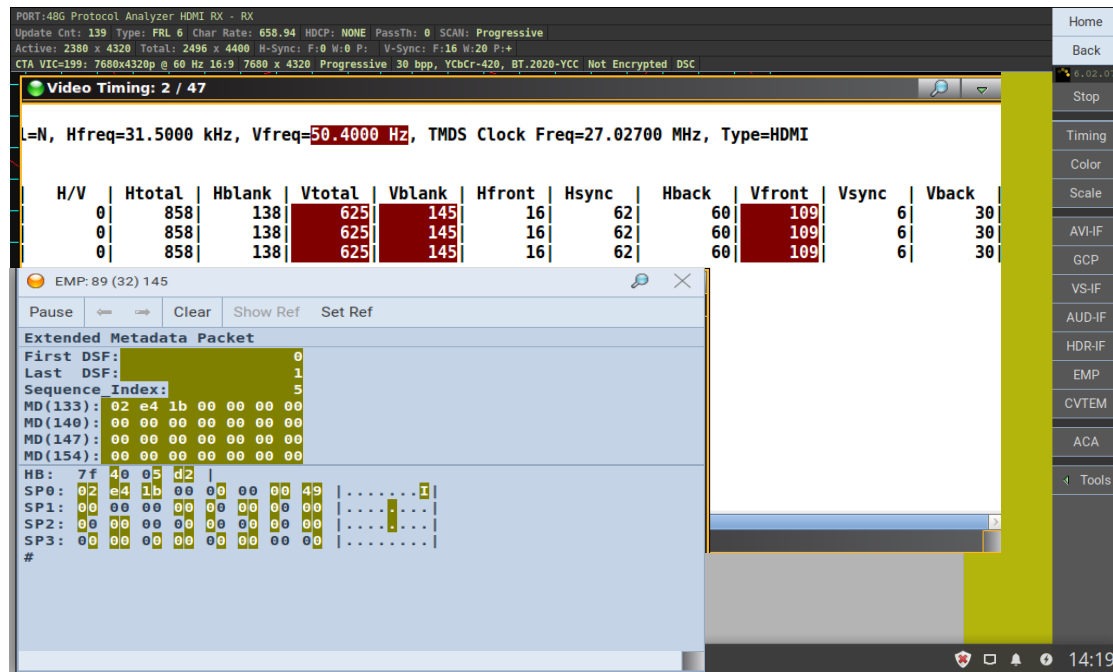
The interface also includes buttons for "Cancel the Compliance Test" and "Pause Test Execution".



# HDMI TMDS Gaming Source Compliance Test

## ◆ HDMI 2.1 TMDS Gaming sink compliance Testing:

- ◆ Run TMDS Gaming sink compliance tests:
  - ◆ Quick Frame Transport (QFT).
  - ◆ Variable Refresh Rate (VRR).
  - ◆ Quick Media Switching (QMS).
  - ◆ VRR with QFT.
  - ◆ ALLM – (Future)
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of TMDS Gaming-capable devices.
- ◆ Enables export of compliance test results to share w/ colleagues.



# Compliance Testing – Export Compliance Test Results

## ◆ HDMI Aux Compliance Test Results Export:

- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.

HTML Viewer

C:\Users\nkendall\Documents\Current\_Work\M4\_980\_Data\_New\A\_DataSet4\frlsrct\results\AA\_XLN\_LT\_MOI\_11\_19\Report\_Cdf.htm

June 2, 2020 8:05 PM [www.quantumdata.com](http://www.quantumdata.com)

### HDMI FRL Source Compliance Test Report

Results Name:	AA_XLN_LT_MOI_11_19	Manufacturer:	xilinx
Date Tested:	October 24, 2018 3:50 PM	Model Name:	hdmi2.1
Overall Status:	Pass	Port Tested:	1

#### Report Index / Summary

Test HFR1-11	Pass	Test HFR1-19	Pass	CDF
<a href="#">Equipment Info</a>				

#### Capabilities Declaration Form (CDF)

General	
CDF_TEST_PERIOD	2000
QD_HP_LENGTH	
QD_LPCM_Modes	
FRL	
Source_Max_FRL_Rate	10 Gbps @ 4 Lanes
Source_Max_TxFE	0
Features	
Source_Supports_4K100A	YES
Source_Supports_4K100B	YES
Source_Supports_4K120A	YES
Source_Supports_4K120B	YES
Source_Supports_8K50A	YES
Source_Supports_8K50B	YES
Source_Supports_8K60A	YES
Source_Supports_8K60B	YES
DSC	
Source_DSC_Max_FRL_Rate	Not Supported

BACK FORWARD SAVE AS... CLOSE



# Compliance Testing – Export Compliance Test Results

## ◆ HDMI Aux Compliance Test Results Export:

- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.

HTML Viewer

C:\Users\nkendall\Documents\Current\_Work\M4\_980\_Data\_New\A\_DataSet4\frlsrct\results\AA\_XLN\_LT\_MOL\_11\_19\Report\_Cdf.htm

<b>Test HFRI-11</b>		Pass
Source FRL Protocol - Legal Codes		
• Iter 01: FRL 3 Lane Mode		Pass
▪ Trained at: (2) 6 Gbps @ 3 Lanes		
• 01: Test that the FRL characters count and SSB/SR characters count is valid.	Pass	
• 02: SR header occurs only after 32 super blocks and at SB count '0'.	Pass	
• 03: Illegal codes or other related errors associated with this test case.	Pass	
• 04: SSB/SR header occurs only prior to Character block '0'.	Pass	
• Iter 02: FRL 4 Lane Mode		Pass
▪ Trained at: (5) 10 Gbps @ 4 Lanes		
• 01: Test that the FRL characters count and SSB/SR characters count is valid.	Pass	
• 02: SR header occurs only after 32 super blocks and at SB count '0'.	Pass	
• 03: Illegal codes or other related errors associated with this test case.	Pass	
• 04: SSB/SR header occurs only prior to Character block '0'.	Pass	

<b>Test HFRI-19</b>		Pass
Source FRL Packets - FRL Map Characters		
• Iter 01: Lowest FRL Rate in 3 Lane mode		Pass
▪ Trained at: (2) 6 Gbps @ 3 Lanes		
• 01: Test that the FRL MAP Type is valid.	Pass	
• 02: Test that Video Blanking/Video Data Characters Length is greater than 1	Pass	
• 03: Test That the sum of all MAP Length fields in a Super Block is 2008.	Pass	
• Iter 02: Lowest FRL Rate in 4 Lane mode		

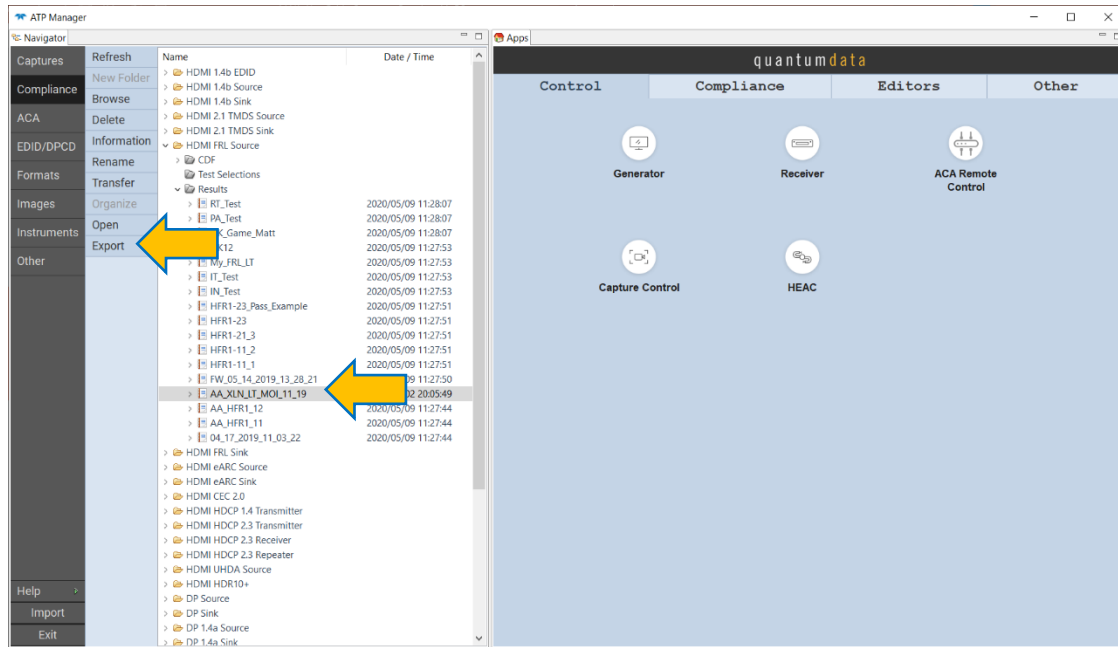
BACK FORWARD

SAVE AS...

CLOSE

# Compliance Testing – Export Compliance Test Results

- ◆ HDMI Aux Compliance Test Results Export:
  - ◆ Save compliance test results and HTML file for easy and universal viewing through browser.
  - ◆ Export compliance test results for dissemination to colleagues, other subject matter experts or Teledyne Customer Support.





# HDMI 2.1 Source Testing

## HDCP Compliance Testing



# HDMI - HDCP 2.3 Source Compliance Testing

- ◆ HDMI HDCP 2.3 compliance Testing:
  - ◆ Run HDCP 2.3 source compliance tests. All tests supported.
  - ◆ Run HDCP 2.3 repeater tests. All tests supported.
  - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
  - ◆ Enables compliance self-testing and/or pre-testing of HDMI devices.
  - ◆ Enables export compliance test results to share with colleagues.

Compliance Test Results Viewer

DP HDCP 2.2 Receiver (1.0) Compliance Test Results

Results Name: AA\_Corn\_Monitor\_1      Manufacturer: LG  
Date Tested: March 15, 2017 7:57 PM      Model Name: 5K Monitor  
Overall Status: **CTS 1.0 - Pass**      Port Tested: 1

HTML Report

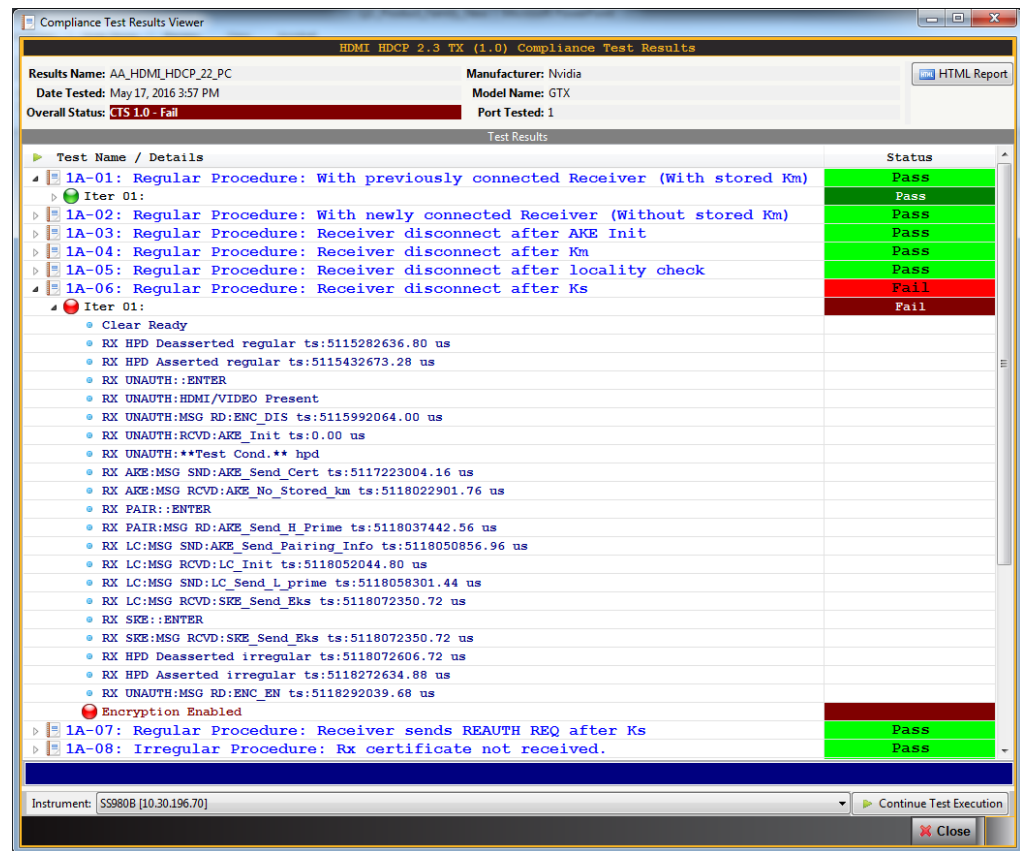
Test Name / Details	Status
2C-01: Regular Procedure - With transmitter	Pass
Iter 01: With previously not connected receiver	Pass
Iter 02: With previously connected receiver	Pass
TX:HPD::ENTER	
TX HPD:**Test Cond.** auth	
TX UNAUTH::ENTER	
TX MSGR:Disable ENC_EN ts:3957204961.28 us	
TX UNAUTH:AKE_INIT ts:3958706882.56 us	
TX UNAUTH:MSG RD:AKE_Init ts:3958706882.56 us	
TX UNAUTH:MSG RCVD:AKE_Send_Cert ts:3958759403.52 us	
TX UNAUTH:Rrx 0,7f,d4,f0,cf,b3,4c,86	
TX UNAUTH:RxCaps 2 0 2	
TX AKE:Snd Stored_RM ts:3958786918.40 us	
TX AKE:MSG:AKE_Stored_km ts:3958786918.40 us	
TX AKE:MSG RCVD:AKE_Send_H_prime ts:3958822830.08 us	
TX LC:Snd LC_Init ts:3958824253.44 us	
TX LC:MSG:LC_Init ts:3958824253.44 us	
TX LC:MSG RCVD:LC_Send_L_prime ts:3958831534.08 us	
TX SKE:Snd SKE_Send_EKS ts:3958833356.80 us	
TX:AUTH::ENTER	
TX AUTH:Snd STRM_TYPE ts:3958843596.80 us 0	
TX MSGR:Enable ENC_EN ts:3959084165.12 us	
TX AUTH:MSG:SKE_Send_Eks ts:0.00 us	
Transmitted test pattern was visible on the Sink DUT.	
2C-02: Irregular Procedure - New Authentication after AKE Init	Pass
2C-03: Irregular Procedure - New Authentication during Locality Check	Pass
2C-04: Irregular Procedure - New Authentication after SKE Send Eks	Pass
2C-05: Irregular Procedure - New Authentication during Link Synchronization	Pass
2C-06: Regular Procedure - Encryption Disable Bootstrapping	Pass

Instrument: SS980B [10.30.196.70]      Continue Test Execution

Close

# HDMI HDCP 2.3 Source Compliance Testing

- ◆ HDMI HDCP 2.3 source compliance Testing:
  - ◆ Run HDCP 2.3 source compliance tests. All tests supported.
  - ◆ Run HDCP 2.3 repeater tests. All tests supported.
  - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
  - ◆ Enables compliance self-testing and/or pre-testing of HDMI devices.
  - ◆ Enables export compliance test results to share with colleagues.



Compliance Test Results Viewer

HDMI HDCP 2.3 TX (1.0) Compliance Test Results

Results Name: AA\_HDMI\_HDCP\_22\_PC Manufacturer: Nvidia  
Date Tested: May 17, 2016 3:57 PM Model Name: GTX  
Overall Status: **CTS 1.0 - Fail** Port Tested: 1

HTML Report

Test Results

Test Name / Details	Status
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	Pass
Iter 01:	Pass
1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	Pass
1A-03: Regular Procedure: Receiver disconnect after AKE Init	Pass
1A-04: Regular Procedure: Receiver disconnect after Km	Pass
1A-05: Regular Procedure: Receiver disconnect after locality check	Pass
1A-06: Regular Procedure: Receiver disconnect after Ks	Fail
Iter 01:	Fail
Clear Ready	
RX HPD Deasserted regular ts:5115282636.80 us	
RX HPD Asserted regular ts:5115432673.28 us	
RX UNAUTH::ENTER	
RX UNAUTH:HDMI/VIDEO Present	
RX UNAUTH:MSG RD:ENC_DIS ts:5115992064.00 us	
RX UNAUTH:RCVD:AKE_Init ts:0.00 us	
RX UNAUTH:**Test Cond.** hpd	
RX AKE:MSG SND:AKE_Send_Cert ts:5117223004.16 us	
RX AKE:MSG RCVD:AKE_No_Stored_km ts:5118022901.76 us	
RX PAIR::ENTER	
RX PAIR:MSG RD:AKE_Send_H_Prime ts:5118037442.56 us	
RX LC:MSG SND:AKE_Send_Pairing_Info ts:5118050856.96 us	
RX LC:MSG RCVD:LC_Init ts:5118052044.80 us	
RX LC:MSG SND:LC_Send_L_prime ts:5118058301.44 us	
RX LC:MSG RCVD:SKE_Send_Eks ts:5118072350.72 us	
RX SKE::ENTER	
RX SKE:MSG RCVD:SKE_Send_Eks ts:5118072350.72 us	
RX HPD Deasserted irregular ts:5118072606.72 us	
RX HPD Asserted irregular ts:5118272634.88 us	
RX UNAUTH:MSG RD:ENC_EN ts:5118292039.68 us	
Encryption Enabled	
1A-07: Regular Procedure: Receiver sends REAUTH REQ after Ks	Pass
1A-08: Irregular Procedure: Rx certificate not received.	Pass

Instrument: SS980B [10.30.136.70] Continue Test Execution

Close

# HDMI HDCP 2.3 Source Compliance Test - ACA Test Capture Logs

## ◆ HDMI Aux Channel Analyzer Timestamp control:

- ◆ View the ACA transaction files for each HDCP test to confirm failures.
- ◆ View details of any transaction.
- ◆ View time stamps.

The screenshot displays the ACA Data Viewer application. The main window shows a list of transactions with columns for line number, transaction type, direction, and timestamp. Transaction 1455 is highlighted. A yellow arrow points from the transaction list to the detailed view on the right.

Line	Type	Direction	Timestamp	Details
1441	DHDCP	DP-R62	+02:04:16.330116	> R:69493 RxStatus L=1
1442	DHDCP	DP-R62	+02:04:16.330188	< ACK 02
1443	DHDCP	DP-R62	+02:04:16.330270	> R:692C0 H' L=8
1444	DHDCP	DP-R62	+02:04:16.330342	< ACK 2D 10 42 F8 9A 0C 34 F8
1445	DHDCP	DP-R62	+02:04:16.330464	> R:692C8 H' (8) L=8
1446	DHDCP	DP-R62	+02:04:16.330536	< ACK 5D 2C 56 B3 A4 17 1F 14
1447	DHDCP	DP-R62	+02:04:16.330657	> R:692D0 H' (16) L=8
1448	DHDCP	DP-R62	+02:04:16.330729	< ACK F7 7E 79 72 4B E6 8E 28
1449	DHDCP	DP-R62	+02:04:16.330851	> R:692D8 H' (24) L=8
1450	DHDCP	DP-R62	+02:04:16.330924	< ACK 73 2D C2 67 66 28 7B 13
1451	DHMSG	DP-R62	+02:04:16.330925	< AKE_Send_H_prime
1452	DHDCP	DP-R62	+02:04:16.331178	> W:692F0 r_n L=8 D9 0C 6F 25 A7 B4 D6 C8
1453	DHDCP	DP-R62	+02:04:16.331313	< ACK
1454	DHMSG	DP-R62	+02:04:16.331313	> LC_Init
1455	DHDCP	DP-T61	+02:04:16.338555	> R:692F8 L' L=8
1456	DHDCP	DP-T61	+02:04:16.338670	< ACK D9 65 19 06 50 D9 B2 70
1457	DHDCP	DP-T61	+02:04:16.338670	> R:69300 L' (8) L=8
1458	DHDCP	DP-T61	+02:04:16.338742	< ACK 3E B3 14 D5 15 B2 CF 01
1459	DHDCP	DP-T61	+02:04:16.338863	> R:69308 L' (16) L=8
1460	DHDCP	DP-T61	+02:04:16.338935	< ACK D4 CE DC 03 CD F3 68 FC
1461	DHDCP	DP-T61	+02:04:16.339057	> R:69310 L' (24) L=8
1462	DHDCP	DP-T61	+02:04:16.339129	< ACK 6F CB A5 A7 7A D3 6D 3F
1463	DHMSG	DP-T61	+02:04:16.339130	< LC_Send_L_prime
1464	DHDCP	DP-T61	+02:04:16.339300	> W:69318 Edkey_Ks L=8 CC DE 03 C0 A9 3...
1465	DHDCP	DP-T61	+02:04:16.339435	< ACK
1466	DHDCP	DP-T61	+02:04:16.339490	> W:69320 Edkey_Ks (8) L=8 4D D3 B2 69 8...
1467	DHDCP	DP-T61	+02:04:16.339624	< ACK
1468	DHDCP	DP-T61	+02:04:16.339679	> W:69328 r_iv L=8 AF 94 4E 79 CA 47 BD E0
1469	DHDCP	DP-T61	+02:04:16.339814	< ACK
1470	DHMSG	DP-T61	+02:04:16.339815	> SKE_Send_Eks
1471	DHDCP	DP-R62	+02:04:16.338477	> R:692F8 L' L=8
1472	DHDCP	DP-R62	+02:04:16.338549	< ACK D9 65 19 06 50 D9 B2 70
1473	DHDCP	DP-R62	+02:04:16.338670	> R:69300 L' (8) L=8
1474	DHDCP	DP-R62	+02:04:16.338742	< ACK 3E B3 14 D5 15 B2 CF 01
1475	DHDCP	DP-R62	+02:04:16.338863	> R:69308 L' (16) L=8
1476	DHDCP	DP-R62	+02:04:16.338935	< ACK D4 CE DC 03 CD F3 68 FC
1477	DHDCP	DP-R62	+02:04:16.339057	> R:69310 L' (24) L=8

The detailed view on the right shows the following information:

- Start Time: +02:04:16.338477
- Type: Native
- Direction: Request
- Command: Read
- Address: 0x692F8 (L')
- Length: 8
- [0000][96 92 F8 07 -- -- --][... ]

The status bar at the bottom shows: 1455: > R:692F8 L' L=8

# HDMI 2.1 eARC Rx Testing

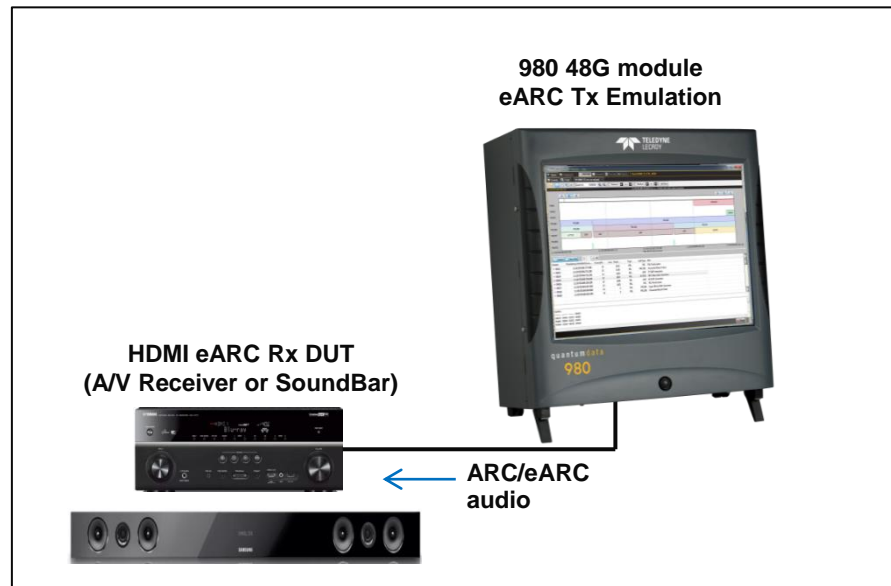
## Enhanced Audio Return Channel





# HDMI eARC Rx Testing

- ◆ HDMI 2.1 eARC Testing:
  - ◆ Verify eARC Rx (e.g. Sound Bar) for common mode and differential mode operation.
  - ◆ Run eARC common and differential mode compliance tests for Rx devices. Full list of tests.



# HDMI eARC Rx Testing

## ◆ HDMI 2.1 eARC Testing:

- ◆ Verify eARC Rx (e.g. Sound Bar) for common mode and differential mode operation.
- ◆ Run eARC common and differential mode compliance tests for Rx devices. Full list of tests supported (only partial list shown right).



# HDMI eARC Rx Testing

## ◆ HDMI 2.1 eARC Testing:

- ◆ Verify eARC Rx (e.g. Sound Bar) for common mode and differential mode operation.
- ◆ Run eARC common and differential mode compliance tests for Rx devices. Full list of tests supported.
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of eARC devices.
- ◆ Enables export of compliance test results to share w/ colleagues.

Compliance Test Results Viewer

eARC Sink (1.0) Compliance Test Results

Results Name: AA\_eARC\_Rx\_Complete\_MB      Manufacturer: Lattice  
Date Tested: August 13, 2018 11:14 AM      Model Name: eval  
Overall Status: **CTS 1.0 - Fail**      Port Tested: 1

Test Results

Test Name / Details	Status
▶ HFR5-2-20: eARC Discovery With COMMA Response Margining	Pass
▶ HFR5-2-21: Command Behavior With Bit Time Margining	Pass
Iter 01:	Pass
01: HFR5 2 21 1: Shortest Bit Time, Earliest Middle Edge	Pass
02: HFR5 2 21 2: Shortest Bit Time, Latest Middle Edge	Pass
03: HFR5 2 21 3: Longest Bit Time, Earliest Middle Edge	Pass
04: HFR5 2 21 4: Longest Bit Time, Latest Middle Edge	Pass
Iteration 4, Longest Bit Time, Latest Middle Edge	
Collecting data for 7000ms	
Collected 2738 events	
Analyzed 2618 events	
TeARC_RX_CONN_START: 20.8082ms (maximum: 200ms)	
COMMA ON #1 was measured at 9.9631ms	
COMMA OFF #1 was measured at 9.9518ms	
COMMA ON #2 was measured at 9.96405ms	
COMMA OFF #2 was measured at 9.951425ms	
COMMA ON #3 was measured at 9.96345ms	
870 packets analyzed	
Re-analyzed 2738 events	
eARC_Read 0x74/0xD2=0x28	
eARC_Write 0x74/0xD3=0x00	
▶ HFR5-2-22: Behavior if no response to eARC Discovery	Pass
▶ HFR5-2-23: eARC RX gets Unexpected Device ID	Pass
▶ HFR5-2-24: eARC RX gets new Opcode in the middle of a Command	Pass
▶ HFR5-2-25: eARC RX gets Heartbeat Disconnect	Pass
▶ HFR5-2-26: eARC RX gets HPD LOW during eARC Discovery	Pass

Open ACA Data      HFR5-2-20: eARC Discovery With COMMA Response Margining

Instrument: SS980B [10.30.196.240]      Continue Test Execution

Close

# HDMI eARC Common Mode Configuration Sequence

## ◆ HDMI 2.1 eARC Testing:

- ◆ Verify eARC common mode connection sequence using Aux Channel Analyzer (ACA) utility.
- ◆ Enables export of ACA eARC Common Mode transactions to share w/ colleagues.

ACA Data Viewer

Open Close Export Options Filter Find

My\_eARC\_Log\_1 Events: 28 (54)

Index	Event	Time	Description
0	EARC HDMI-R10	+06:37:28.021241	Invalid Sequence
1	EARC HDMI-R10	+06:37:28.069262	Read EARC_RX_STAT 00
2	EARC HDMI-R10	+06:37:28.069813	Write EARC_TX_STAT 81
3	EARHB HDMI-R10	+06:37:28.116296	Heartbeats 166
4	SV HDMI-R10	+06:37:36.078772	SV Falling Edge
5	SV HDMI-R10	+06:37:37.884404	SV Rising Edge
6	EARCM HDMI-R10	+06:37:37.885490	Comma CN: 9.999 ms
7	EARCM HDMI-R10	+06:37:37.905489	Comma CN: 10.000 ms
8	EARCM HDMI-R10	+06:37:37.925489	Comma CN: 10.000 ms
9	EARC HDMI-R10	+06:37:37.939303	Read EARC_RX_STAT 18
10	EARC HDMI-R10	+06:37:37.939853	Write EARC_TX_STAT 99
11	EARHB HDMI-R10	+06:37:37.985256	Heartbeats 1
12	EARC HDMI-R10	+06:37:38.033313	Read EARC_RX_STAT 00
13	EARC HDMI-R10	+06:37:38.033860	Write EARC_TX_STAT 81
14	EARC HDMI-R10	+06:37:38.081215	Read CAPS 00h L=8
15	EARCD HDMI-R10	+06:37:38.082492	Cap Data: L=8
16	EARC HDMI-R10	+06:37:38.082526	Read ERX_LATENCY 00
17	EARHB HDMI-R10	+06:37:38.083075	Heartbeats 27
18	EARC HDMI-R10	+06:37:39.392340	Read EARC_RX_STAT 00
19	EARC HDMI-R10	+06:37:39.392909	*Write EARC_TX_STAT 81
20	EARHB HDMI-R10	+06:37:39.440367	Heartbeats 37
21	EARC HDMI-R10	+06:37:41.228225	Read EARC_RX_STAT 00
22	EARC HDMI-R10	+06:37:41.228761	Write EARC_TX_STAT
23	EARHB HDMI-R10	+06:37:41.277215	Heartbeats 43
24	EARC HDMI-R10	+06:37:43.341254	Read EARC_RX_STAT 00
25	EARC HDMI-R10	+06:37:43.341835	Write EARC_TX_STAT
26	EARHB HDMI-R10	+06:37:43.389271	Heartbeats 83
27	EARC HDMI-R10	+06:37:47.396808	Write

Type: eArc  
Start Time: +06:37:38.033313  
Duration: 514 us

Read EARC\_RX\_STAT 00

0xD0: EARC\_RX\_STAT

Bit	Name	Value	Description
0	EARC_HPD	N(0)	
1		0	Reserved
2		0	Reserved
3	CAP_CHNG	N(0)	
4	STAT_CHNG	N(0)	
5		0	Reserved
6		0	Reserved
7		0	Reserved

Packet Sequence:

Index	Event	Time	Description
001:	M C 01h Read	+0 us	
002:	S C 04h Ack	+24 us	
003:	M D 74h	+34 us	
004:	S C 04h Ack	+24 us	
005:	M D D0h	+34 us	
006:	S C 04h Ack	+24 us	
007:	M C 10h Cont	+31 us	
008:	S D 00h	+24 us	
009:	M C 20h Stop	+34 us	
010:	S C 04h Ack	+24 us	

(M/S = Master/Slave, C/D = Command/Data)

12: Read EARC\_RX\_STAT 00

# HDMI 2.1 Sink Testing Video Generation





# HDMI 2.1 Video Generator Function – Select Resolution and Color Parameters

- ◆ HDMI Video Generator:
  - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.

Generator

Modes MODE:FRL FRL:4/10G FMT:4320p60 F-Rate:1485.00MHz F-Rate:60.00Hz Output

(199) 7680x4320p @ 60 Hz 16:9 IMG:SmpteBar 7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc

Format Pattern Audio Tools

CTA VESA Folder Lists EDID

Resolution		Vtotal		Frame Rate		Aspect Ratio
240p2x	240p4x	262	263	24/1.001	24	4:3
288p2x	288p4x	312	313		25	16:9
480p		314		30/1.001	30	64:27
480p2x	480i2x			48/1.001	48	256:135
480p4x	480i4x				50	
576p				60/1.001	60	Box
576p2x	576i2x				100	FILL
576p4x	576i4x			120/1.001	120	4:3
720p					200	16:9
1080p	1080i	1125	1250	240/1.001	240	1.85:1
	4320p					2.39:1

Left to Right Settings Edit Clear Selection

CLOSE

# HDMI 2.1 Video Generator Function – Select Resolution and Color Parameters

- ◆ HDMI Video Generator:
  - ◆ Test 4K UHD TVs with a variety of video formats and video parameters.
  - ◆ Use variety of test patterns including moving patterns to check motion artifacts.
  - ◆ Extensive video format library with the ability to create custom formats.

The screenshot shows the 'Generator' application window. At the top, it displays 'Modes' and various technical specifications: MODE:FRL, FRL:4/10G, FMT:4320p60, P-Rate:1485.00MHz, F-Rate:60.00Hz, INTF:HDMI, DSC:No, IMG:SmpteBar, H-Rate:264.00kHz, and Output. Below this is a table with columns for Format, Pattern, Audio, and Tools. The 'Format' column is expanded, showing a list of video formats. A yellow arrow points to the '4320p60 VIC 199' format. To the right, a 'Format Settings' dialog box is open, showing 'Color Space' options (RGB, YCbCr, xvYCC, opRGB) and 'Range' options (Full, Shoot, Limited). A yellow arrow points to the '4:2:0' color format. Below the 'Range' section, the 'Bits per Component' section shows options for 8, 10, 12, and 16 bits, with a yellow arrow pointing to the '10' option. At the bottom, the 'Scrambling Override' section shows a toggle switch set to 'Off' and an 'APPLY' button.

Resolution	Total	Frame Rate
240p2x	262	24/1.001
240p4x	263	24
288p2x	312	25
288p4x	313	25
480p	314	30/1.001
480p2x		30
480i2x		48/1.001
480p4x		48
480i4x		50
576p		60/1.001
576p2x		60
576i2x		100
576p4x		120/1.001
576i4x		120
720p		240/1.001
1080p	1125	240
1080i	1250	1.85:1
2160p		2.39:1

# HDMI TMDS Video Generation – Configure Outgoing Metadata

- ◆ HDMI Video Generator:
  - ◆ Test 4K UHD TVs with a variety of video formats and video parameters.
  - ◆ Enables user control over Infoframe and data island transmission for irregular testing.

The screenshot shows the 'Generator' application window. At the top, it displays modes: MODE: FRL, FRL: 4/10G, FMT: 4320p60, F-Rate: 1485.00MHz, F-Rate: 60.00Hz, INTF: HDMI, DSC: No, IMG: SmpteBar, H-Rate: 264.00kHz. Below this, it shows (199) 7680x4320p @ 60 Hz 16:9, 7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc. The interface has several tabs: Format, Pattern, Audio, Tools, and a right-hand panel with Disconnect, Refresh, eARC Master TX, and 48G Generator HDMI. The 'Tools' tab is highlighted with a yellow arrow. The 'InfoFrame' tab is also highlighted with a yellow arrow. The 'InfoFrame' tab shows various settings: EDID Decode, EDID Comp, AVI, SDCS Editor, HDR, Link Train, DSC, HDMI, LLC, 3D, HDMI, Forum, AFC, SPD, Image Ctrl, CEC Ping, CEC Tester, UHDA Test, HDR Lab, HDR10+, Dolby Vision, Editors, and Scripts. The 'AVI' sub-tab is active, showing Video Format ID (VIC): 0 (0 - 255). Other settings include Component Format (Y): 0 = RGB, AFD Present (A): 0 = No, Bar Data (B): 0 = Not Present, Scan Info (S): 1 = Overscanned, Colorimetry (C): 1 = SMPTE 170M [1], Picture Aspect Ratio (M): 0 = No Data, Active Aspect Ratio (R): 0 = Not Specified, ITC Content (ITC): 0 = No Data, Ext. Colorimetry (EC): 0 = xvYCC601, RGB Quantization (Q): 0 = Default, Picture Scaling (SC): 0 = None, YCC Quantization (YQ): 0 = Limited Range, IT Content Type (CN): 0 = Graphics, Pixel Repetition (PR): 0 = No Repetition (x1), and Add. Colorimetry Ext (ACE): 0 = DCL-P3 R'G'B' (D65). At the bottom, there is a table with columns T, V, L, C, Params 1, VIC, Params 2, AFD, and Params 3. The table contains data for VIC 014000 and AFD 00000000000000000000.

# HDMI Video Generator Function

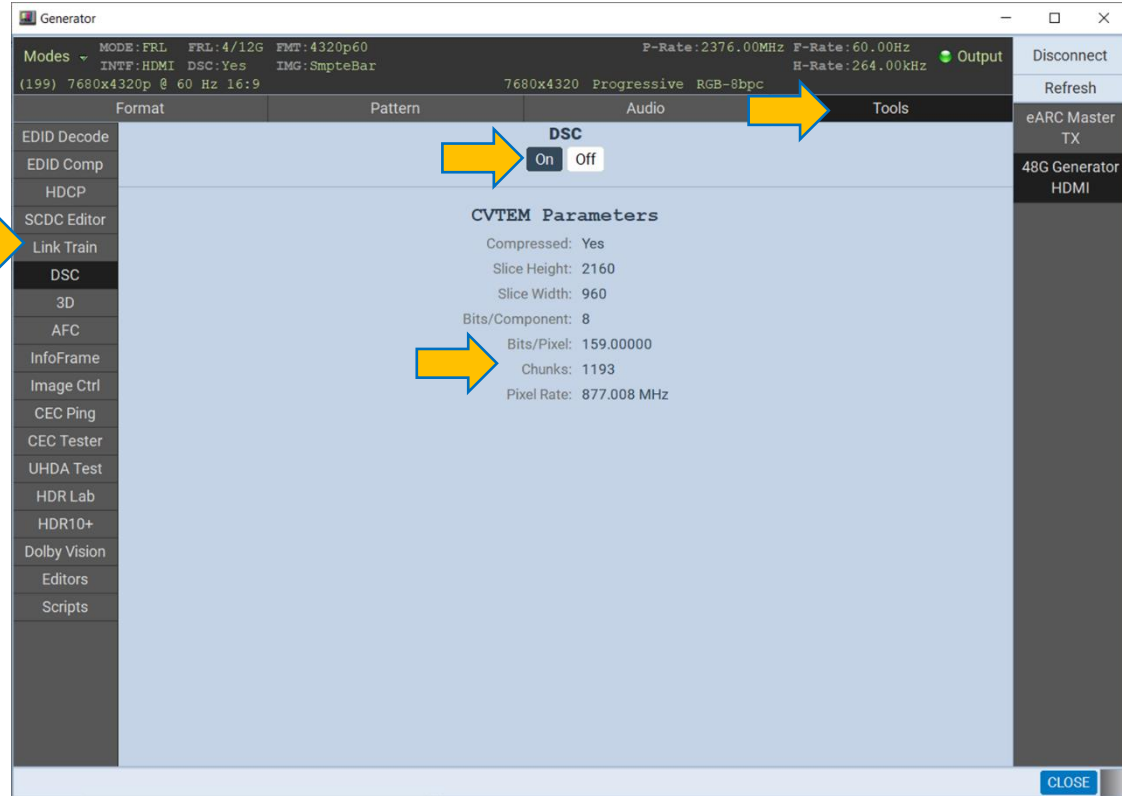
- ◆ HDMI Video Generator:
  - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
  - ◆ Configure Link settings with Lane rate & number of Lanes.
  - ◆ Turn FRL Off to test TMDS.

The screenshot shows the 'Generator' application window. The top status bar displays: MODE: FRL, FRL: 4/10G, FMT: 4320p60, F-Rate: 1485.00MHz, F-Rate: 60.00Hz, INTF: HDMI, DSC: No, IMG: SmpteBar, H-Rate: 264.00kHz, Output (green dot), and Disconnect. Below this, it shows (199) 7680x4320p @ 60 Hz 16:9, 7680x4320 Progressive, YCbCr-420: BT.2020, VCC-10bpc. The main interface has four tabs: Format, Pattern, Audio, and Tools. The Tools tab is selected and highlighted with a yellow arrow. On the left, a vertical menu lists various functions: EDID Decode, EDID Comp, HDCP, SCDC Editor, Link Train (highlighted with a yellow arrow), DSC, 3D, AFC, InfoFrame, Image Ctrl, CEC Ping, CEC Tester, UHDA Test, HDR Lab, HDR10+, Dolby Vision, Editors, and Scripts. The 'Current Status' section shows: State: LTS\_P, Lanes: 4, Rate: 10 GHz, FFE: 0, and FRL PLL LOCKED: YES. The 'Force Link Train at' section has a sub-header 'Lane / Rate' and a list of options: FRL Off, 3 Lanes / 3 Gbps, 3 Lanes / 6 Gbps, 4 Lanes / 6 Gbps, 4 Lanes / 8 Gbps, 4 Lanes / 10 Gbps (highlighted with a yellow arrow), and 4 Lanes / 12 Gbps. On the right side, there are buttons for Disconnect, Refresh, eARC Master TX, and 48G Generator HDMI. A 'CLOSE' button is at the bottom right.

# HDMI Video Generator Function – Selecting DSC

## ◆ HDMI Video Generator:

- ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
- ◆ Configure Link settings with Lane rate & number of Lanes.
- ◆ Turn FRL Off to test TMDS.
- ◆ You can active Display Stream Compression (DSC) when the 980 48G module is in the FRL video generation mode.





# HDMI Video Generator Function – DSC Image Caching

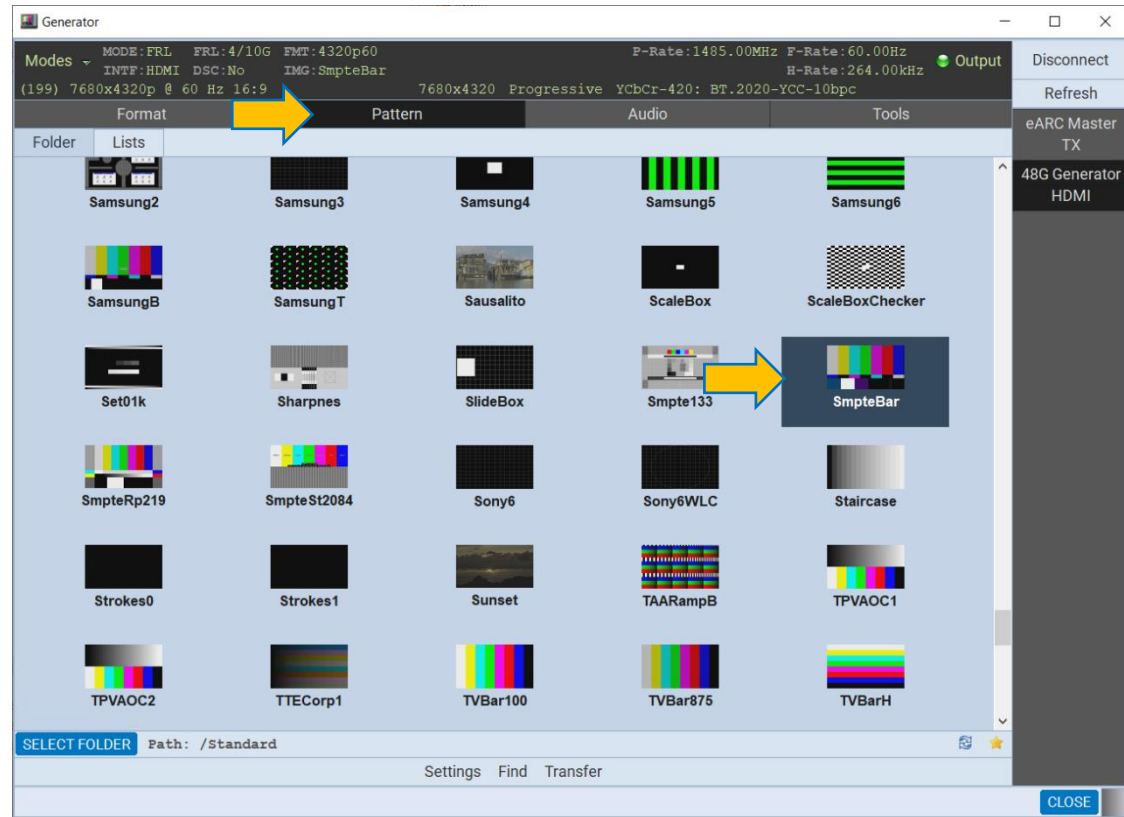
- ◆ HDMI Video Generator – DSC Image Caching:
  - ◆ Install or create cached, pre-compressed DSC images for quick rendering.

The screenshot displays the HDMI Video Generator software interface. On the left is a vertical menu with options: Link Train, HDCP, EDID Decode, EDID Comp, SDC Editor, **DSC**, 3D, AFC, InfoFrame, Image Shift, Image Ctrl, CEC Ping, CEC Tester, UHD-A Test, HDR Lab, HDR10+, Dolby Vision, Editors, and Scripts. The 'DSC' option is highlighted with a yellow arrow. The main window is divided into several tabs: Format, Pattern, DSC, Audio, and Tools. The 'DSC' tab is active, showing a list of 32 DSC images. Each entry includes a number, a label (e.g., Master), and technical specifications (e.g., 3840x2160, VCMF 4:2:0, 10 bpc, Slice 1520x2160, 24 bpc). A yellow arrow points to the 'ADD CURRENT DSC IMAGE TO THE CACHE' button at the top of the list. Another yellow arrow points to the 'Cache' tab in the top right corner of the main window.

# HDMI Video Generator Function – Test Pattern Selection

## ◆ HDMI Video Generator:

- ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
- ◆ Includes a variety of test patterns and special patterns for testing UHD displays.
- ◆ Verify HDR rendering capabilities of a 8K UHD TV.



# HDMI Video Generator Function – HDR Test Patterns

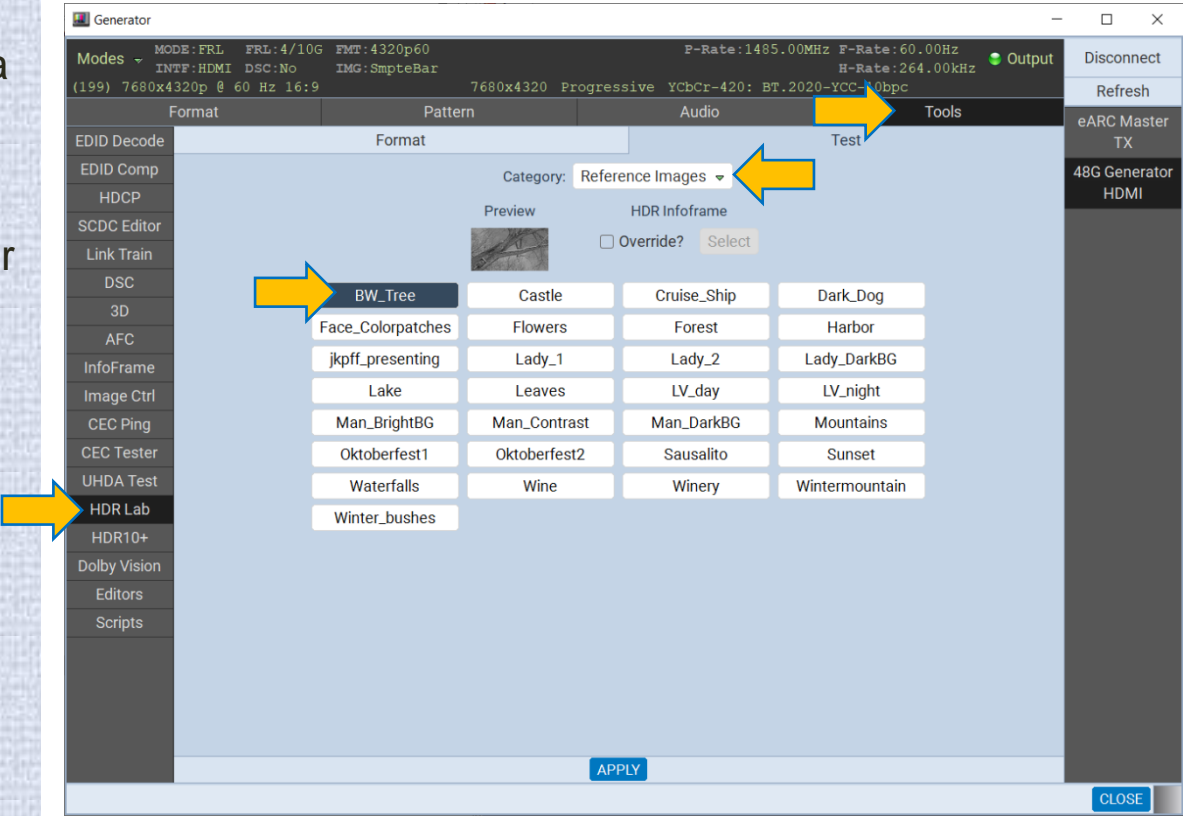
- ◆ HDMI Video Generator:
  - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
  - ◆ Includes a variety of test patterns and special patterns for testing UHD displays.
  - ◆ Verify HDR rendering capabilities of a 8K UHD TV.

The screenshot shows the 'Generator' application window. On the left, a vertical menu lists various functions: EDID Decode, EDID Comp, HDCP, SCDC Editor, Link Train, DSC, 3D, AFC, InfoFrame, Image Ctrl, CEC Ping, CEC Tester, UHDA Test, **HDMI Lab** (highlighted with a yellow arrow), HDR10+, Dolby Vision, Editors, and Scripts. The main area displays the 'Format' tab, which is titled 'Select a 2160p/BT2020 Mode'. It features a table of video modes with columns for RGB, YCC-420, YCC-422, and YCC-444, and rows for different refresh rates (23 Hz, 24 Hz, 25 Hz, 29 Hz, 30 Hz). A 'Depth' dropdown on the right is set to '10 bpc'. At the bottom of the main area is an 'APPLY' button. The top status bar shows various settings: MODE: FRL, FRL: 4/10G, FMT: 4320p60, P-Rate: 1485.00MHz, F-Rate: 60.00Hz, INTF: HDMI, DSC: No, IMG: SmpteBar, H-Rate: 264.00kHz, and Output status. On the far right, there are buttons for Disconnect, Refresh, eARC Master TX, 48G Generator HDMI, and a CLOSE button at the bottom right.

RGB	YCC-420	YCC-422	YCC-444
23 Hz	50 Hz	23 Hz	50 Hz
24 Hz	59 Hz	24 Hz	59 Hz
25 Hz	60 Hz	25 Hz	60 Hz
29 Hz		29 Hz	29 Hz
30 Hz		30 Hz	30 Hz

# HDMI Video Generator Function – HDR Test Patterns

- ◆ HDMI Video Generator:
  - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
  - ◆ Includes a variety of test patterns and special patterns for testing UHD displays.
  - ◆ Verify HDR rendering capabilities of a 8K UHD TV.



# HDMI Video Generator Function – HDR Test Patterns

## ◆ HDMI Video Generator:

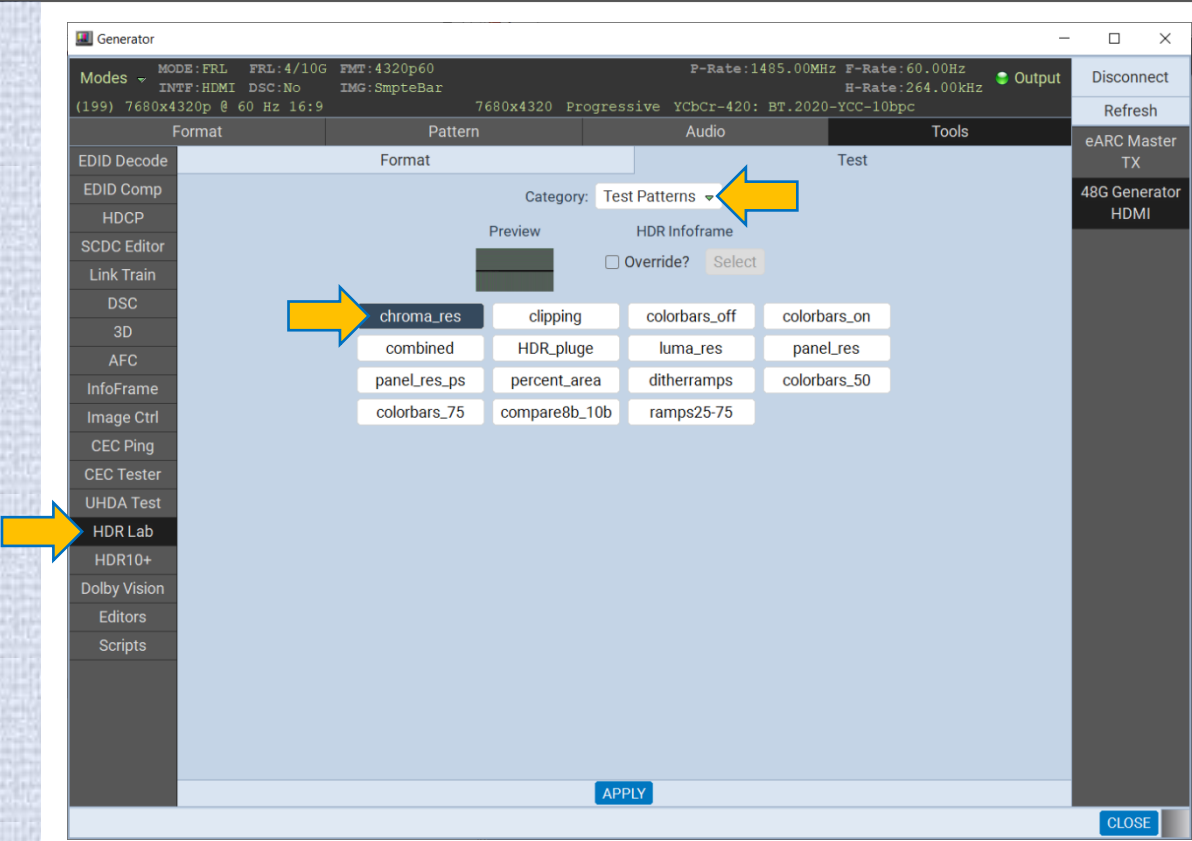
- ◆ Test 4K and 8K UHD TVs for HDR10 with a variety of video formats and colorimetry settings.
- ◆ Includes a variety of test patterns and special natural images (shown) for testing UHD displays.
- ◆ Verify HDR rendering capabilities of 4K and 8K UHD TV for HDR10 subjectively.





# HDMI TMDS and FRL Video Generation – HDR Lab

- ◆ HDMI Video Generator:
  - ◆ Test 4K UHD TVs with a variety of video formats and video parameters.
  - ◆ Verify HDR rendering capabilities of a 4K UHD TV.





# HDMI FRL Video Generation – HDR Lab

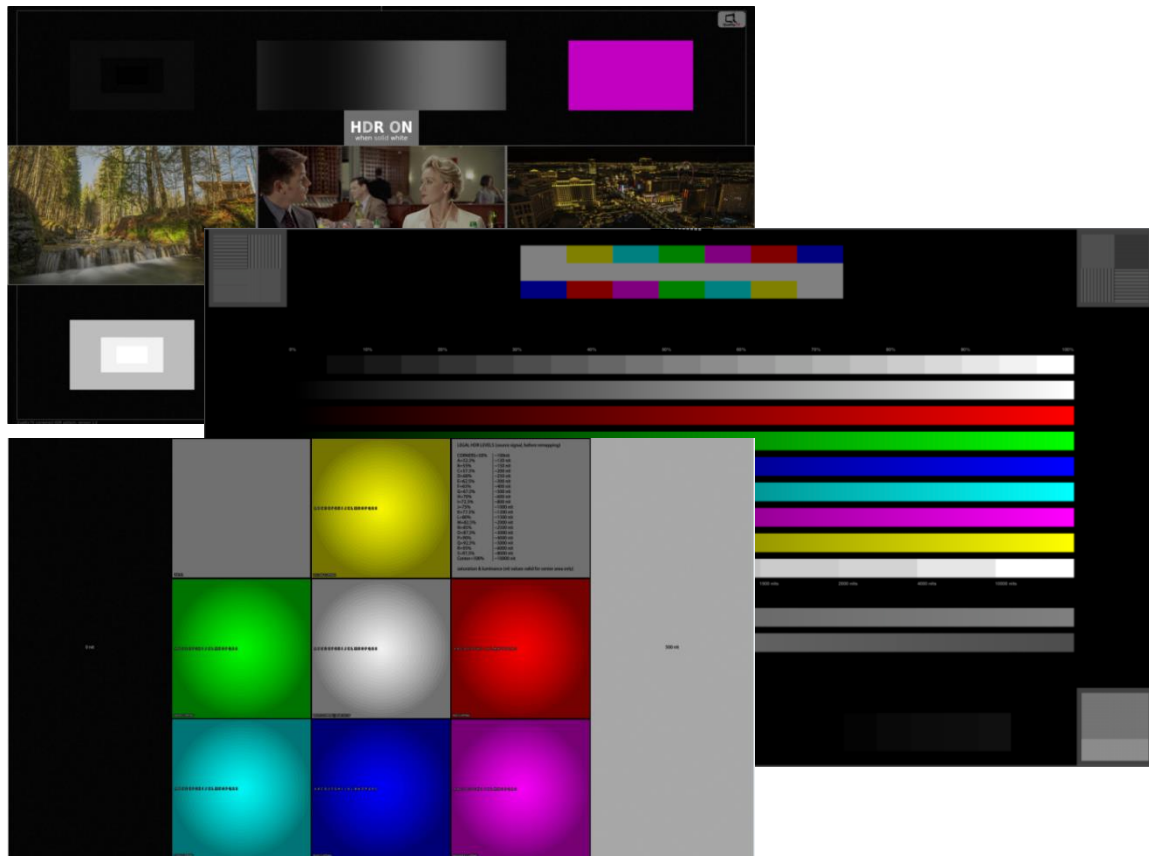
- ◆ HDMI Video Generator:
  - ◆ Test 8K UHD TVs with a variety of video formats and video parameters.
  - ◆ Verify HDR rendering capabilities of a 8K UHD TV.

The screenshot displays the 'HDR Lab' interface within the HDMI FRL Video Generation software. The left sidebar lists various tools, with 'HDR Lab' highlighted by a yellow arrow. The main configuration area shows the 'Format' tab selected, displaying a list of video formats. A yellow arrow points to the 'Amsterdam\_HDR\_8k' button in the 'Pattern' section. The 'Preview' window shows a street scene, and the 'APPLY' button is at the bottom.



# HDMI 2.1 Video Generator Function – HDR Test Patterns

- ◆ HDMI Video Generator:
  - ◆ Test 4K and 8K UHD TVs for HDR10 with a variety of video formats and colorimetry settings.
  - ◆ Includes a variety of HDR test patterns (shown) and special natural images for testing UHD displays.
  - ◆ Verify HDR rendering capabilities of 4K and 8K UHD TV for HDR10 objectively.



# HDMI Sink Testing

## Custom Formats and Format Lists

# Video Generator – Custom Format Timing

## ◆ HDMI Video Generator:

- ◆ Create custom video timings for testing a display's response to a variety of standard and non-standard or irregular timings.
- ◆ Save custom timings in separate list for easy access and testing.
- ◆ Create custom format lists of standard formats, e.g. 8K formats.

Format Editor: /User/My\_Format

New Open Save Use

Timing General Digital Video Digital Audio AFD

☒ Calculated

Pixel Rate ☒ 25.200000 MHz 39.682540 ms

	Horizontal		Vertical	
Rate	<input type="text" value="31.500000"/> KHz		<input type="text" value="60.000000"/> Hz	
Active	<input type="text" value="640"/> Pixels <input checked="" type="checkbox"/>	<input type="text" value="25.396825"/> us	<input type="text" value="480"/> Lines <input checked="" type="checkbox"/>	<input type="text" value="15.238095"/> ms
Blank	<input type="text" value="160"/> Pixels <input type="checkbox"/>	<input type="text" value="6.349206"/> us	<input type="text" value="45"/> Lines <input type="checkbox"/>	<input type="text" value="1.428571"/> ms
Total	<input type="text" value="800"/> Pixels <input checked="" type="checkbox"/>	<input type="text" value="31.746032"/> us	<input type="text" value="525"/> Lines <input checked="" type="checkbox"/>	<input type="text" value="16.666667"/> ms
Pulse Delay	<input type="text" value="16"/> Pixels <input type="checkbox"/>	<input type="text" value="0.634921"/> us	<input type="text" value="10"/> Lines <input type="checkbox"/>	<input type="text" value="0.317460"/> ms
Pulse Width	<input type="text" value="96"/> Pixels <input type="checkbox"/>	<input type="text" value="3.809524"/> us	<input type="text" value="2"/> Lines <input type="checkbox"/>	<input type="text" value="0.063492"/> ms

Serration width Adjustment  Pixels

H to V Pulse Delay  Pixels

Horizontal Broad Pulse Delay  Pixels

Eq. Before  Lines

Eq. After  Lines

Entry Units

☒ Machine

☐ Time

Scan Type

☒ Progressive

☐ Interlace

☐ Back Porch

☐ Clock Pulse

☐ PreEmphasis

☐ DC Balance

☐ Flat Front Porch

☐ TriLevel

☐ Repeat Field

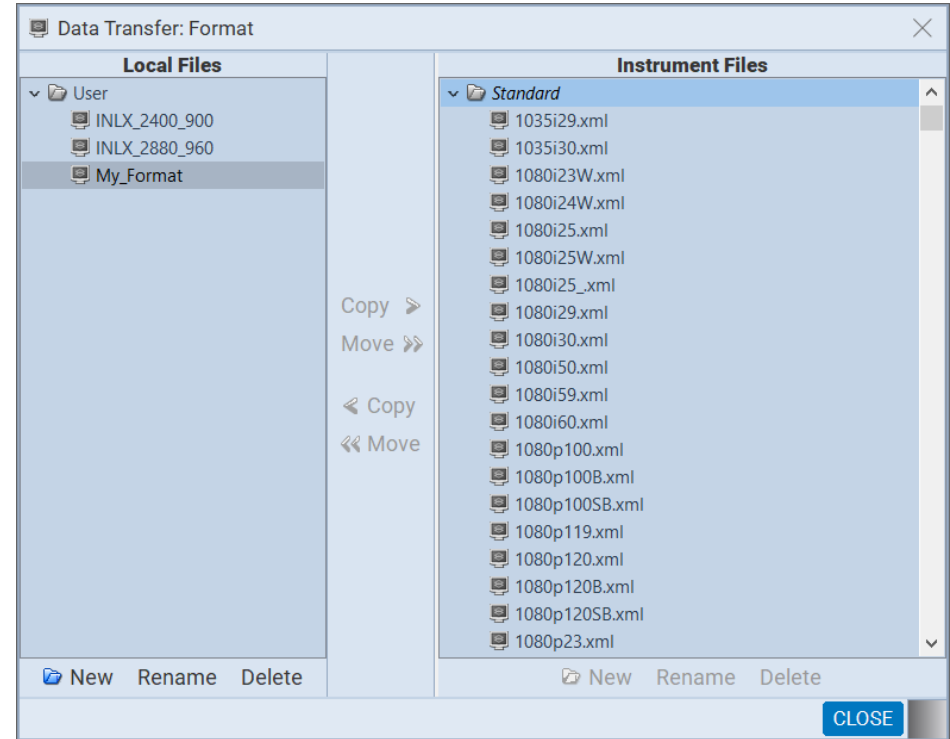
CLOSE



# Video Generator – Custom Format Timing

## ◆ HDMI Video Generator:

- ◆ Create custom video timings for testing a display's response to a variety of standard and non-standard or irregular timings.
- ◆ Save custom timings in separate list for easy access and testing.
- ◆ Create custom format lists of standard formats, e.g. 8K formats.



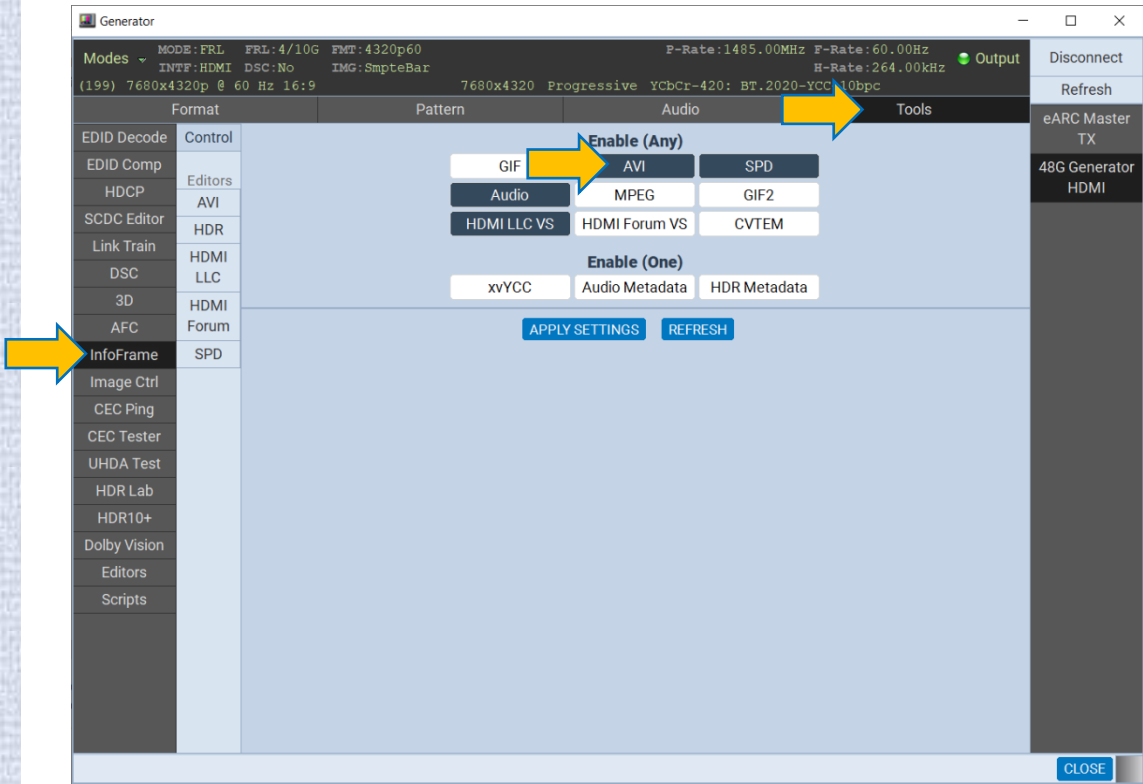
# HDMI Sink Testing InfoFrame and Data Island Editor





# HDMI Video Generator – InfoFrame Output Control

- ◆ HDMI Video Generator:
  - ◆ Configure HDMI InfoFrame parameter values to test sink response to irregular conditions.
  - ◆ Examples show AVI InfoFrame and HDR InfoFrame.



# HDMI Video Generator – InfoFrame Output Control

- ◆ HDMI Video Generator:
  - ◆ Configure HDMI InfoFrame parameter values to test sink response to irregular conditions.
  - ◆ Example shows AVI InfoFrame.
  - ◆ Use Pull-Down menus to make changes to outgoing AVI InfoFrame.

The screenshot shows the 'Generator' application window. At the top, it displays various settings: MODE: FRL, FRL: 4/10G, FMT: 4320p60, F-Rate: 1485.00MHz, F-Rate: 60.00Hz, INTF: HDMI, DSC: No, IMG: SmpteBar, H-Rate: 264.00kHz, and Output status. Below this, it shows the video format: (199) 7680x4320p @ 60 Hz 16:9, 7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc.

The main interface is divided into several sections: Format, Pattern, Audio, and Tools. The 'Format' section is active, showing a list of InfoFrame types on the left: EDID Decode, EDID Comp, AVI, HDR, DSC, 3D, AFC, InfoFrame, Image Ctrl, CEC Ping, CEC Tester, UHDA Test, HDR Lab, HDR10+, Dolby Vision, Editors, and Scripts. The 'AVI' option is selected, and a yellow arrow points to it. The 'InfoFrame' section is expanded, showing a list of parameters with pull-down menus. A yellow arrow points to the 'Colorimetry (C):' menu, which is currently set to '2 = ITU-R BT.709 [7]'. Other parameters include Component Format (Y), AFD Present (A), Bar Data (B), Scan Info (S), Picture Aspect Ratio (M), Active Aspect Ratio (R), ITC Content (ITC), Ext. Colorimetry (EC), RGB Quantization (Q), Picture Scaling (SC), YCC Quantization (YQ), IT Content Type (CN), and Pixel Repetition (PR).

At the bottom, there is a table for 'Add. Colorimetry Ext (ACE):' with columns T, V, L, C, Params 1, VIC, Params 2, AFD, and Params 3. The table contains the following data:

T	V	L	C	Params 1	VIC	Params 2	AFD	Params 3
82	02	0D	EF	008000	00	00	000000000000000000	
				Reserved				
00	00000000000000000000000000000000							

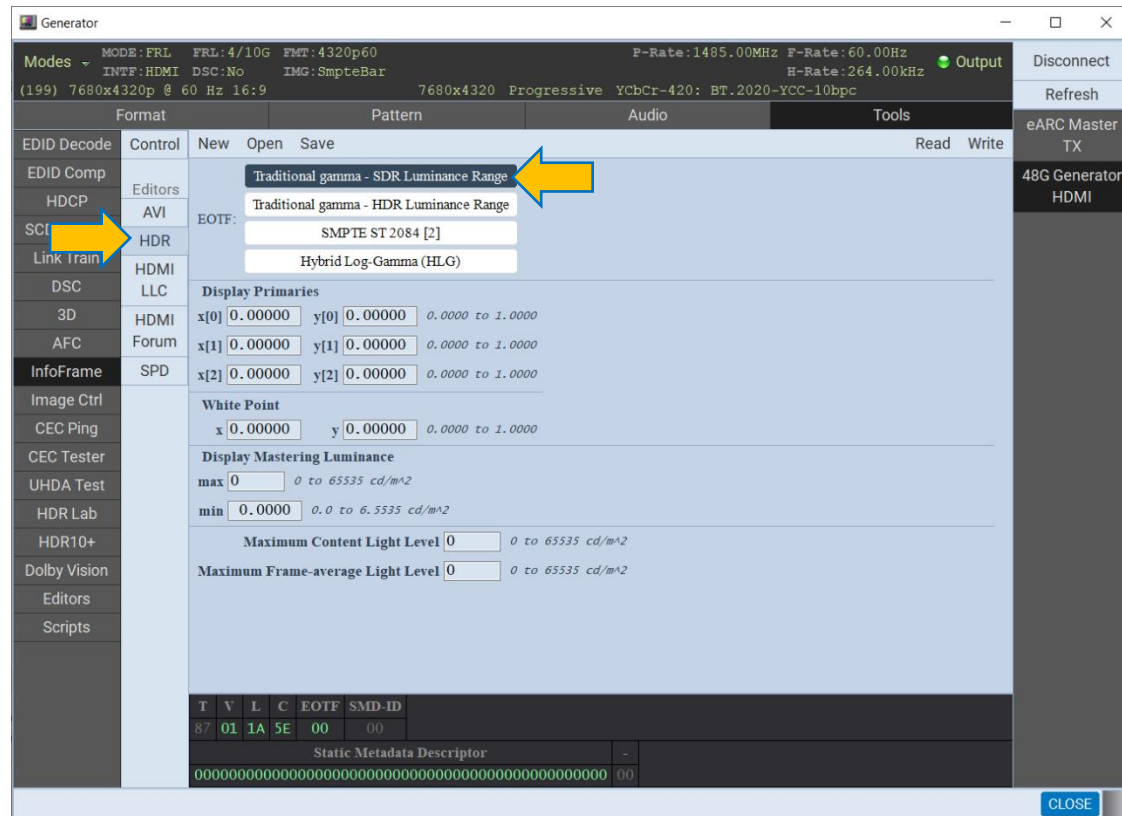
The 'CLOSE' button is located at the bottom right of the window.



## Video Generator – HDMI Inframe Output Control

## ◆ HDMI Video Generator:

- ◆ Configure HDMI InfoFrame parameter values to test sink response to irregular conditions.
- ◆ Examples shows HDR InfoFrame.
- ◆ Use fields to enter HDR parameters to outgoing HDR InfoFrame.



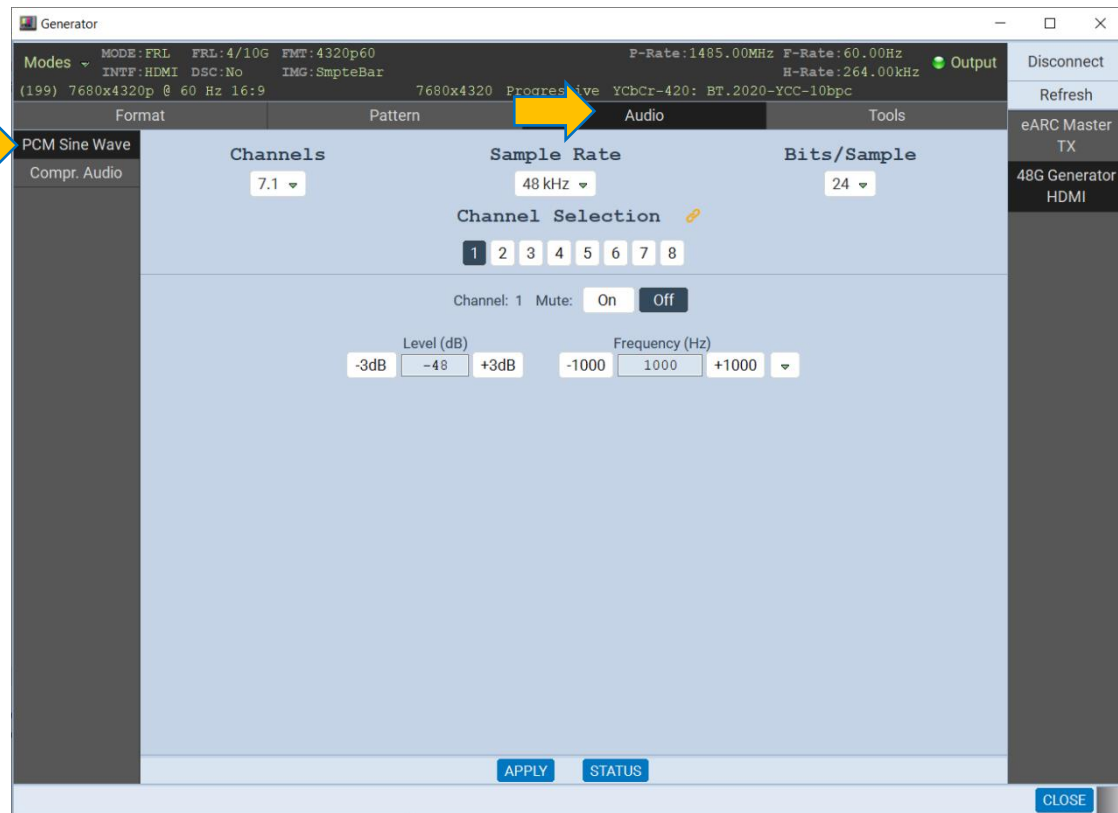
# HDMI 2.1 Sink Testing Audio Generation



# HDMI Audio Generator – LPCM Configuration

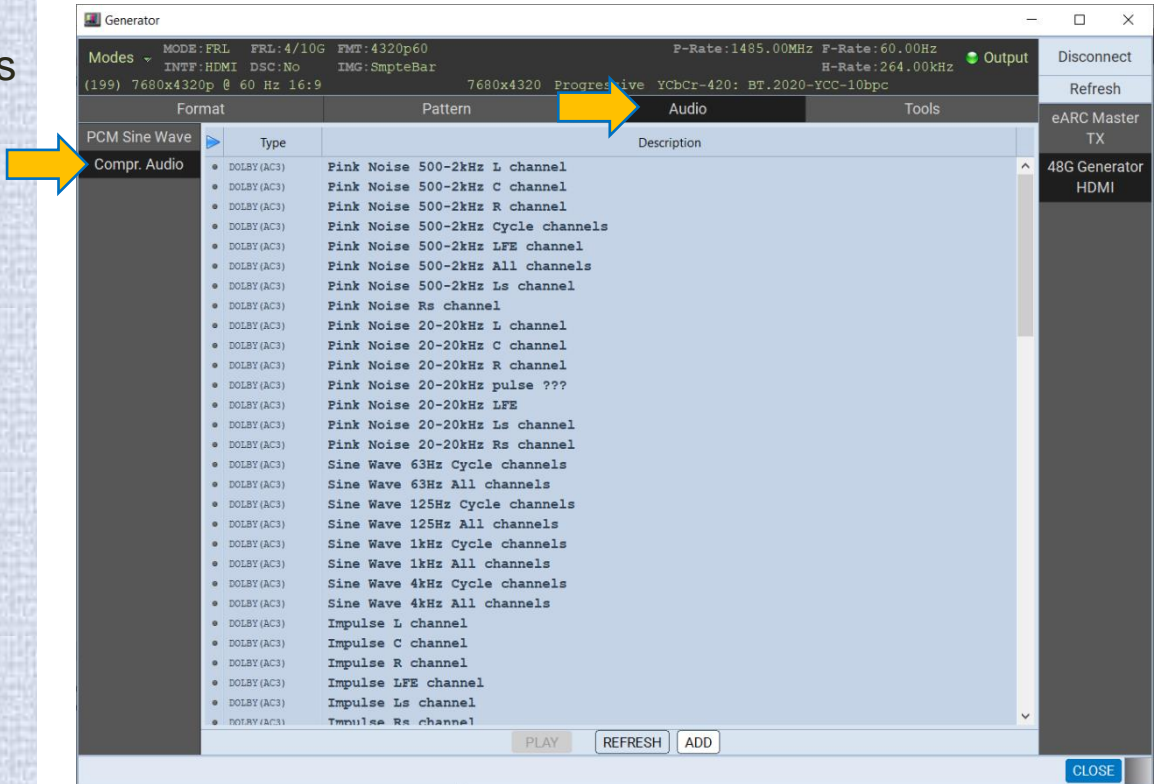
## ◆ HDMI Audio Generator:

- ◆ Test UHD TVs and A/V receivers with a variety of audio formats.
- ◆ Specify LPCM audio parameters in the sine wave such as number of channels, sampling rate, bits per pixel, and sine wave amplitude and frequency.



# HDMI Audio Generator – Compressed Formats

- ◆ HDMI Audio Generator:
  - ◆ Test UHD TVs and A/V receivers with a variety of audio formats.
  - ◆ Select from a variety of compressed audio clips.
  - ◆ Provides Dolby and DTS audio clips for replay.





# HDMI 2.1 Sink Testing

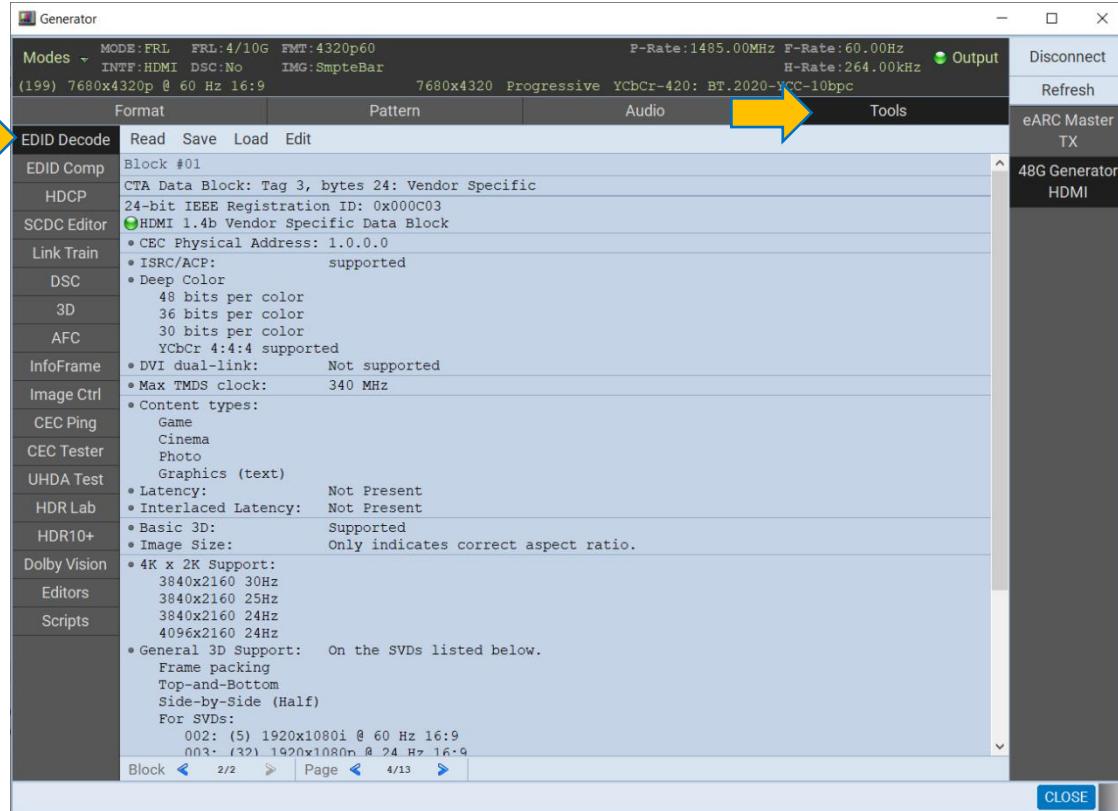
## EDID and SCDC Testing



# HDMI Video Generator – EDID Decode and Verification

## ◆ HDMI Video Generator:

- ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
- ◆ Verify EDID and SCDC register content of connected display.



# HDMI Video Generator – EDID Decode with DSC

- ◆ HDMI Video Generator:
  - ◆ Test 4K and 8K UHD TVs with a variety of video formats and colorimetry settings.
  - ◆ Verify EDID and SCDC register content of connected display.
  - ◆ The example shows that the sink EDID is showing support for Display Stream Compression (DSC).



**Generator**

Modes: FRL:4/12G FMT:4320p60 F-Rate:2376.00MHz F-Rate:60.00Hz Output  
INTF:HDMI DSC:No IMG:SmpteBar H-Rate:264.00kHz  
(199) 7680x4320p @ 60 Hz 16:9 7680x4320 Progressive RGB-8bpc

Format Pattern Audio Tools

**EDID Decode** Read Save Load Edit

Block #01

HDCP CTA Data Block: Tag 3, bytes 13: Vendor Specific  
24-bit IEEE Registration ID: 0xC45DD8

SCDC Editor HDMI Forum Vendor Specific Data Block

Link Train  
\* Version: 1  
\* Max TMDs Character Rate: 600 MHz  
\* Max FRL Rate: 12 Gbps @ 4 Lanes

DSC  
Y: SCDC Present  
N: RR\_Capable  
N: CABLE\_STATUS  
N: CCBPCI  
Y: LTE\_340MHz\_scramble  
N: Independent\_view  
N: Dual\_View  
N: 3D\_OSD\_Disparity  
N: UHD\_VIC  
Y: DC\_48bit\_420  
Y: DC\_36bit\_420  
Y: DC\_30bit\_420

3D  
AFC  
InfoFrame  
Image Ctrl  
CEC Ping  
CEC Tester  
UHDA Test  
HDR Lab  
HDR10+  
Dolby Vision

Editors  
Scripts  
\* VRRmin: 0 Hz  
\* VRRMax: 0 Hz  
Y: DSC\_10bpc  
Y: DSC\_12bpc  
Y: DSC\_16bpc  
Y: DSC\_1p2  
Y: DSC\_All\_bpp  
Y: DSC\_Native\_420  
\* DSC\_Max\_FRL\_Rate: 12 Gbps  
\* DSC\_MaxSlices: Up to 16 slices and up to (400 MHz/KSliceAdjust) pixel clock per slice  
\* DSC\_TotalChunkKBytes: 63 = 65536 bytes

Block 2/2 Page 5/11

CLOSE



# HDMI Video Generator – Compare EDIDs

- ◆ HDMI Video Generator:
  - ◆ View and verify EDID contents of a connected display. Check for checksum and header errors
  - ◆ Check EDID against known-reference or read the same EDID successively.
  - ◆ Report provides details difference.

Generator

MODE:FRL FRL:4/10G FMT:4320p60 F-Rate:1485.00MHz F-Rate:60.00Hz Output Disconnect  
INTF:HDMI DSC:No IMG:SmpteBar H-Rate:264.00kHz  
(199) 7680x4320p @ 60 Hz 16:9 7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc

Format Pattern Audio Tools

EDID Decode  
EDID Comp  
HDCP  
SCDC Editor  
Link Train  
DSC  
3D  
AFC  
InfoFrame  
Image Ctrl  
CEC Ping  
CEC Tester  
UHDA Test  
HDR Lab  
HDR10+  
Dolby Vision  
Editors  
Scripts

Select the EDIDs to Compare

Two Sink Reads Sink vs EDID #2 EDID #1 vs EDID #2

Edid #1 Select Read from Sink

Edid #2 Select 1200MHz\_10G

COMPARE

The EDIDs are different.

#1: Read from Sink #2: 1200MHz\_10G

Block 2/2

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	02	03	59	14	F0	59	52	10	05	20	22	04	03	02	07	06
10	5F	60	61	62	64	65	66	C2	23	C4	0F	C3	7E	7E	03	7D
20	7F	00	07	F8	78	03	12	F0	C1	C8	00	18	1A	10	01	16
30	04	00	81	56	41	58	00	16	17	06	08	08	5D	00	C4	48
40	78	7F	88	00	67	00	E2	1E	00	0F	4B	E3	83	06	7F	07
50	C5	10	E3	58	06	12	0F	12	01	00	E3	BA	05	88	FF	12
60	50	1A	30	29	20	50	35	30	00	20	BA	35	88	00	21	1A
70	00	1A	1E	51	30	00	46	1E	8F	13	33	46	00	0F	BA	33

DECODE AND DIFF

# Video Generator – Verify SCDC Registers

- ◆ HDMI Video Generator:
  - ◆ Read and verify HDMI SCDC register values for capabilities, configuration and status.



Generator

Modes

MODE:FRL FRL:4/10G FMT:4320p60 P-Rate:1485.00MHz F-Rate:60.00Hz Output

INTF:HDMI DSC:No IMG:SmpteBar H-Rate:264.00kHz

(199) 7680x4320p @ 60 Hz 16:9 7680x4320 Progressive YCbCr-420: BT.2020-YCC-10bpc

Format

Pattern

Audio

Tools

EDID Decode

Version

EDID Comp

HDCP

Update Flags

SCDC Editor

Configuration

Link Train

DSC

Status Flags

3D

AFC

Character Error Detection

InfoFrame

Test

Image Ctrl

Configuration

CEC Ping

Manufacturer Specific

CEC Tester

UHDA Test

HDR Lab

HDR10+

Dolby Vision

Editors

Scripts

READ ALL

READ PAGE

REPORT

Status Flags

Bit 3: 0 1 Rsvd (0)

Bit 4: 0 1 Rsvd (0)

Bit 5: 0 1 Rsvd (0)

Bit 6: 0 1 Rsvd (0)

Bit 7: 0 1 Rsvd (0)

0x40 (R) Status\_0

Bit 0: 0 1 Clock Detected

Bit 1: 0 1 Ch0\_Ln0\_Locked

Bit 2: 0 1 Ch1\_Ln1\_Locked

Bit 3: 0 1 Ch2\_Ln2\_Locked

Bit 4: 0 1 Lane3\_Locked

Bit 5: 0 1 Reserved

Bit 6: 0 1 FLT\_Ready

Bit 7: 0 1 DSC\_DecodeFail

0x41 (R) Status\_1

Bits 0-3: Ln0\_LTP\_req 0: No Pattern Requested

Bits 4-7: Ln1\_LTP\_req 0: No Pattern Requested

WRITE ALL

WRITE PAGE

CLOSE

Disconnect

Refresh

eARC Master TX

48G Generator HDMI




# HDMI 2.1 Sink Testing Compliance Testing



# HDMI Fixed Rate Link (FRL) Sink Compliance Test

## ◆ HDMI 2.1 FRL sink compliance Testing:

- ◆ Run FRL sink compliance tests.  
Full list of tests supported (partial list shown right).



The screenshot shows a software window titled "FRL Sink" with a menu bar containing "Instrument: AL\_M41d [10.30.196.30]", "Connect", and "Cards". Below the menu bar are three tabs: "CDF Entry", "Test Selection", and "Test Options / Preview". The "Test Selection" tab is active, displaying a list of tests. At the top right of the test list is a green button labeled "EXECUTE TESTS". At the bottom right is a blue button labeled "CLOSE".

Select All	✓	✗	
▼			<b>CED</b>
▶			HFR2-17: Sink FRL Protocol - CED - Lock Bits
▶			HFR2-18: Sink FRL Protocol - CED - Error Counting During Reads
▶			HFR2-19: Sink FRL Protocol - CED - Specific Video Data Error Injection
▶			HFR2-20: Sink FRL Protocol - CED - Maximum Video Data Error Injection
▶			HFR2-21: Sink FRL Protocol - CED - Update Flag with Specific Error Injection
▶			HFR2-22: Sink FRL Protocol - CED - Update Flag with Maximum Error Injection
▼			<b>RS</b>
▶			HFR2-48: Sink FRL Protocol - RS - Basic Operation
▶			HFR2-49: Sink FRL Protocol - RS - Correction Counting During Reads
▶			HFR2-50: Sink FRL Protocol - RS - Maximum Symbol Error Count
▶			HFR2-51: Sink FRL Protocol - RS - Update Flag with Specific Symbol Error Count
▶			HFR2-52: Sink FRL Protocol - RS - Update Flag with Maximum Symbol Error Count
▼			<b>8bpc Decoding</b>
▶			HFR2-23: Sink Pixel Decoding (FRL Mode) - YCBCR 4:2:0
▶			HFR2-31: Sink Pixel Decoding (FRL Mode) - RGB
▶			HFR2-32: Sink Pixel Decoding (FRL Mode) - YCBCR 4:2:2/4:4
▼			<b>DC Decoding</b>
▶			HFR2-24: Pixel Decoding (FRL Mode) - YCbCr 4:2:0 Deep Color
▶			HFR2-33: Sink Pixel Decoding (FRL Mode) - Non-YCbCr 4:2:0 Deep Color
▼			<b>8bpc Timing</b>
▶			HFR2-11: Sink Video Timing (FRL Mode) - Sub-2160p 24-bit Color Depth
▶			HFR2-12: Sink Video Timing (FRL Mode) - 2160p 24-bit Color Depth
▶			HFR2-13: Sink Video Timing (FRL Mode) - 4320p 24-bit Color Depth
▼			<b>DC Timing</b>
▶			HFR2-14: Sink Video Timing (FRL Mode) - Sub-2160p Deep Color
▶			HFR2-15: Sink Video Timing (FRL Mode) - 2160p Deep Color
			HFR2-30: Audio Decoding and Rendering (FRL Mode) - MS Audio (L-PCM and 61937) - Sample Packet



# HDMI Fixed Rate Link (FRL) Sink Compliance Test

## ◆ HDMI 2.1 FRL sink compliance Testing:

- ◆ Run FRL sink compliance tests. Full list of tests supported.
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of FRL devices.
- ◆ Enables export of compliance test results to share w/ colleagues.

Compliance Test Results Viewer

FRL Sink (2.1b) Compliance Test Results

Results Name: AA\_NVK\_RS\_48\_Full  
Date Tested: December 11, 2018 11:14 AM  
Overall Status: **CIS 2.1b - Fail**

Manufacturer: gd  
Model Name: 980  
Port Tested: 1

HTML Report

Test Name / Details	Status
HFR2-48: Sink FRL Protocol - RS - Basic Operation	Pass
Iter 01: 3 Lanes	Pass
Iter 02: 4 Lanes	Pass
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 4. Read the RSCC, verify that RS C Valid flag = 0; otherwise FAIL.	Fail
0xA8:59/5A 0:80	
Sink RS_C_Valid flags not 0 80	
0xA8:59/5A 0:80	
Sink RS_C_Valid flags not 0 80	
03: 7. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all ac	Pass
04: 8. Read the FRL Start flag. Repeat until FRL Start is set (=1), else FAIL after	Pass
05: 10. Read the RSCC, verify that RS C Valid flag = 1 and count = 0 or 1; otherwise	Pass
06: 11. Corrupt symbols at a rate of about 1e-9, spaced out over 10 seconds, with 1	Pass
07: 12. Read the RSCC; if the value is not correct within 1 count then FAIL.	Pass
08: 13. Read the RSCC again after 100 milliseconds; if the count is not 0 or 1 then	Pass
09: 14. Corrupt symbols at a rate of about 2e-9, spaced out over 10 seconds, with 2	Pass
10: 15. Read the RSCC; if the value is not correct within 1 count then FAIL.	Pass
11: 16. Corrupt one symbol in each of 4 consecutive RS blocks, after generating the	Pass
12: 17. Change the FRL data stream to be random data on all lanes.	Pass
13: 18. After 5 seconds, read each FRL Lock bit and verify that they have all been c	Pass
14: 19. Read the RSCC, verify that RS C Valid flag = 1; otherwise FAIL	Pass
15: 20. If the count in the RSCC is less than 4, then FAIL.	Pass
HFR2-49: Sink FRL Protocol - RS - Correction Counting During Reads	Fail
Iter 01:	Fail
01: 1. CDF field Source Max FRL Rate is 0 then skip the test.	Pass
02: 2. Perform Link Training at the minimum FRL Rate with the maximum number of FRL	Pass
03: 4. Read each FRL Lock bit. Repeat until all FRL Lock bits are set (=1) on all ac	Pass
04: 7. Read the RSCC, verify that RS C Valid flag = 1 and count = 0 or 1; otherwise F	Pass
05: 8. Corrupt one symbol in each of a known random number (between 10000 and 30000)	Pass
06: 9. 100 milliseconds after the start of the symbol error, read the RSCC and add t	Pass
07: 11.1. If the correction count is outside the range of ±2 from the number of gene	Fail
HFR2-50: Sink FRL Protocol - RS - Maximum Symbol Error Count	Pass
HFR2-51: Sink FRL Protocol - RS - Update Flag with Specific Symbol Error Count	Pass
HFR2-52: Sink FRL Protocol - RS - Update Flag with Maximum Symbol Error Count	Pass

HFR2-48: Sink FRL Protocol - RS - Basic Operation

Instrument: S5980B [10.30.196.240]

Continue Test Execution

Close



# HDMI TMDS Sink Compliance Test

## ◆ HDMI TMDS compliance Testing:

- ◆ Run TMDS sink compliance tests. Full list of tests supported (partial list shown right).



# HDMI TMDS Sink Compliance Test

- ◆ HDMI TMDS compliance Testing:
  - ◆ Run TMDS sink compliance tests. Full list of tests supported.
  - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
  - ◆ Enables compliance self-testing and/or pre-testing of HDMI TMDS devices.
  - ◆ Enables export of compliance test results to share with colleagues.

The screenshot shows a software window titled "Compliance Test Results Viewer". The main content area displays "HDMI 2.0 Sink (2.0) Compliance Test Results". Key information includes:

- Results Name:** Test\_ID\_2-5\_1
- Date Tested:** May 22, 2014 10:45 AM
- Overall Status:** CTS 2.0 - Pass (highlighted in green)
- Manufacturer:** ACME
- Model Name:** XYZ
- Port Tested:** 1

A button labeled "HTML Report" is visible in the top right. Below this, a section titled "Test Results" contains a table:

Test Name / Details	Status
HF2-5: TMDS Protocol - 6G - Scrambling	Pass
Iter 01:	Pass
• Test Format: (97) 3840x2160p @ 60 Hz 16:9, 24 bpp	
• Scrambling_Status bit was set to 1.	
• Manual inspection of the DUT verified adequate support of the	

At the bottom, there is a field for "Instrument: 980B\_MKC [192.168.254.161]" and a "Continue Test Execution" button. A "Close" button is in the bottom right corner.



# HDMI TMDS Sink Compliance Test

- ◆ HDMI TMDS compliance Testing:
  - ◆ Run TMDS sink compliance tests. Full list of tests supported.
  - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
  - ◆ Enables compliance self-testing and/or pre-testing of HDMI TMDS devices.
  - ◆ Enables export of compliance test results to share with colleagues.

The screenshot displays the 'Compliance Test Results Viewer' application window. The title bar reads 'Compliance Test Results Viewer'. The main content area is titled 'HDMI 2.0 Sink (2.0) Compliance Test Results'. It shows test details for 'Test\_ID\_2-9\_1' performed on 'May 22, 2014 12:08 PM' by 'Manufacturer: ACME' and 'Model Name: XYZ'. The 'Overall Status' is 'CTS 2.0 - Pass' and 'Port Tested: 1'. A table lists test results, including 'HF2-9: TMDS Protocol - Scrambling <= 340Msc' which passed, and its subtests 'Iter 01:' and '01: (2) 720x480p @ 60 Hz 4:3, Not Scrambled', both of which also passed. The interface includes a 'HTML Report' button, a 'Continue Test Execution' button, and a 'Close' button.

Test Name / Details	Status
HF2-9: TMDS Protocol - Scrambling <= 340Msc	Pass
Iter 01:	Pass
01: (2) 720x480p @ 60 Hz 4:3, Not Scrambled	Pass

# HDMI FRL/TMDS Gaming Sink Compliance Test

- ◆ HDMI 2.1 FRL/TMDS Gaming sink compliance Testing:
  - ◆ Run FRL/TMDS Gaming sink compliance tests:
    - ◆ Quick Frame Transport (QFT).
    - ◆ Variable Refresh Rate (VRR).
    - ◆ Quick Media Switching (QMS).
    - ◆ VRR with QFT.
    - ◆ ALLM (not currently supported).
  - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
  - ◆ Enables compliance self-testing and/or pre-testing of FRL or TMDS Gaming-capable devices.
  - ◆ Enables export of compliance test results to share w/ colleagues.

The screenshot displays the 'Compliance Test Results Viewer' window. The title bar reads 'Compliance Test Results Viewer'. The main window has a header 'FRL Sink (2.1b) Compliance Test Results'. Below this, there is a summary section with the following information:

- Results Name: Gaming\_Sink\_Sample
- Date Tested: October 7, 2019 4:54 PM
- Overall Status: **CIS 2.1b - Pass**
- Manufacturer:
- Model Name:
- Port Tested: 1

There is an 'HTML Report' button in the top right corner. Below the summary, there is a table titled 'Test Results' with two columns: 'Test Name / Details' and 'Status'.

Test Name / Details	Status
▶ <b>HF2-60: Quick Frame Transport for Sinks</b>	<b>Pass</b>
▶ Iter 01: 720p60 (or other suitable Format)	<b>Pass</b>
▶ Format: (4) 1280x720p @ 60 Hz 16:9	
▶ 01: FF=1, no VTEms	<b>Pass</b>
▶ 02: FF=2	<b>Pass</b>
▶ 03: FF=1 with VTEms	<b>Pass</b>
▶ 04: FF=2, wait 5s, FF=1 no VTEms	<b>Pass</b>
▶ 05: FF=MAX (if not 2)	<b>Pass</b>
▶ Iter 02: All other supported Formats	<b>Pass</b>
▶ <b>HF2-61: Variable Refresh Rate for Sinks</b>	<b>Pass</b>
▶ Iter 01: Step 4: EDID Checks	<b>Pass</b>
▶ Iter 02: Step 5: 1080p60, Static VRR=48	<b>Pass</b>
▶ Iter 03: Step 5: 3840x2160p60, Static VRR=48	<b>Pass</b>
▶ Iter 04: Step 5: 2560x1440@60, Static VRR=48	<b>Skipped</b>
▶ Iter 05: Step 6: 1080p60, Static VRR=VRRmin	<b>Pass</b>
▶ Iter 06: Step 6: 3840x2160p60, Static VRR=VRRmin	<b>Pass</b>
▶ Iter 07: Step 6: 2560x1440@60, Static VRR=VRRmin	<b>Skipped</b>
▶ Iter 08: Step 7: 1080p120, Static VRR=VRRmin/100/VRRmax	<b>Skipped</b>
▶ Iter 09: Step 7: 3840x2160p120, Static VRR=VRRmin/100/VRRmax	<b>Skipped</b>
▶ Iter 10: Step 7: 2560x1440@120, Static VRR=VRRmin/100/VRRmax	<b>Skipped</b>
▶ Iter 11: Step 8: 1080p60, Dynamic VRR, ignore Mdelta	<b>Pass</b>
▶ Iter 12: Step 8: 3840x2160p60, Dynamic VRR, ignore Mdelta	<b>Pass</b>
▶ Iter 13: Step 8: 2560x1440@60, Dynamic VRR, ignore Mdelta	<b>Skipped</b>
▶ Iter 14: Step 9: 1080p60, Dynamic VRR, honor Mdelta	<b>Pass</b>
▶ <b>HF2-62: Quick Media Switching for Sinks</b>	<b>Pass</b>
▶ <b>HF2-63: VRR with QFT for Sinks</b>	<b>Pass</b>

At the bottom of the window, there is an 'Instrument' dropdown menu showing 'SS980B [10.30.196.70]' and a 'Continue Test Execution' button. There is also a 'Close' button in the bottom right corner.



# HDMI Compliance Testing – Export Compliance Test Results

## ◆ HDMI Aux Compliance Test Results Export:

- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.

HTML Viewer  
C:\Users\inkendall\Documents\Current\_Work\Marketing\PSG\_WW\_Sales\April\_2018\QD\_Resources\980\_Practice\_Utility\980mgr\frsinkct\results\My\_FRL\_Sink\_CT\_Test\_1\Report\_Cdf.htm

April 12, 2019 11:24 AM [www.quantumdata.com](http://www.quantumdata.com)

### HDMI FRL Sink Compliance Test Report CTS 2.1b

Results Name:	My_FRL_Sink_CT_Test_1	Manufacturer:	ACME
Date Tested:	April 11, 2019 1:57 PM	Model Name:	XYZ
Overall Status:	Incomplete	Port Tested:	1

Capabilities Declaration Form (CDF)	
FRL	
Sink_Max_FRL_Rate	12 Gbps @ 4 Lanes
Sink_Supports_ALLM	NO
Sink_Supports_VRR	NO
Sink_Supports_DSC	NO
Features	
Sink_Supports_4K100A	NO
Sink_Supports_4K100B	NO
Sink_Supports_4K120A	NO
Sink_Supports_4K120B	NO
Sink_Supports_8K50A	NO
Sink_Supports_8K50B	NO
Sink_Supports_8K60A	NO
Sink_Supports_8K60B	NO
DSC	
Sink_Supports_DSC	NO
6G - Video	

Back Forward Save As Close



# HDMI Compliance Testing – Export Compliance Test Results

## ◆ HDMI Aux Compliance Test Results Export:

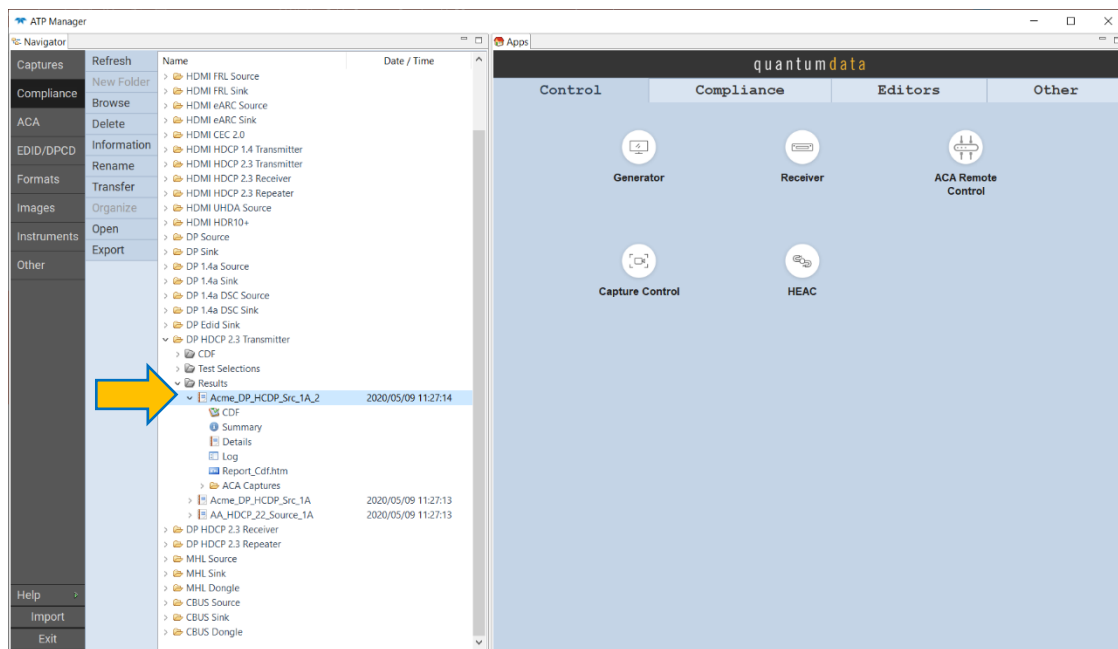
- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.

HTML Viewer	
C:\Users\kendall\Documents\Current_Work\Marketing\PSG_WW_Sales\April_2018\QD_Resources\980_Practice_Utility\980mgr\frtsinkct\results\My_FRL_Sink_CT_Test_1\Report_Cdf.htm	
Test HFR2-17 Sink FRL Protocol - CED - Lock Bits	Incomplete
• Iter 01: 3 Lanes	User Skipped
• Iter 02: 4 Lanes	Pass
• 01: 1. CDF field Source_Max_FRL_Rate is 0 then skip the test.	
• Cable Connected. link trained for 4 lanes 3 rate.	
• 02: 3. Read the EDID after HPD is asserted.	
• 03: 4. Read each FRL Lock bit. If any FRL Lock bits are set (~1), then FAIL.	
• 04: 7. Read each FRL Lock bit after 10 milliseconds. If any FRL Lock bits are cleared (=0) on any active Lanes, then FAIL.	
• 4 lanes, testing lane(0xF=all):0xf, FRL LOCK bits:0x5e exp:0xf mask:0xf	
• 05: 8. Read the FRL_Start flag after 200 milliseconds. If FRL_Start is not set (~1), then FAIL.	
• 06: 11. Read the FRL Lock bit for Lane 0 after 10 milliseconds, verify that the bit is still set (~1). If the FRL Lock bit has cleared (=0), then FAIL.	
• 4 lanes, testing lane(0xF=all):0x0, FRL LOCK bits:0x5e exp:0x1 mask:0x1 4 lanes, testing lane(0xF=all):0x1, FRL LOCK bits:0x5e exp:0x2 mask:0x2 4 lanes, testing lane(0xF=all):0x2, FRL LOCK bits:0x5e exp:0x4 mask:0x4 4 lanes, testing lane(0xF=all):0x3, FRL LOCK bits:0x5e exp:0x8 mask:0x8	
• 07: 13. After at least 2 Super Blocks, read Lane 0 Lock bit and verify it has been cleared (=0). If the FRL Lock bit is set (~1), then FAIL.	
• 4 lanes, testing lane(0xF=all):0x0, FRL LOCK bits:0x5e exp:0x0 mask:0x1 4 lanes, testing lane(0xF=all):0x1, FRL LOCK bits:0x5e exp:0x0 mask:0x2 4 lanes, testing lane(0xF=all):0x2, FRL LOCK bits:0x5e exp:0x0 mask:0x4 4 lanes, testing lane(0xF=all):0x3, FRL LOCK bits:0x4e exp:0x0 mask:0x8	
Save	
Back Forward Save As Close	

# HDMI Compliance Testing – Export Compliance Test Results

## ◆ HDMI Aux Compliance Test Results Export:

- ◆ Save compliance test results and HTML file for easy and universal viewing through browser.
- ◆ Export compliance test results for dissemination to colleagues, other subject matter experts or Teledyne Customer Support.



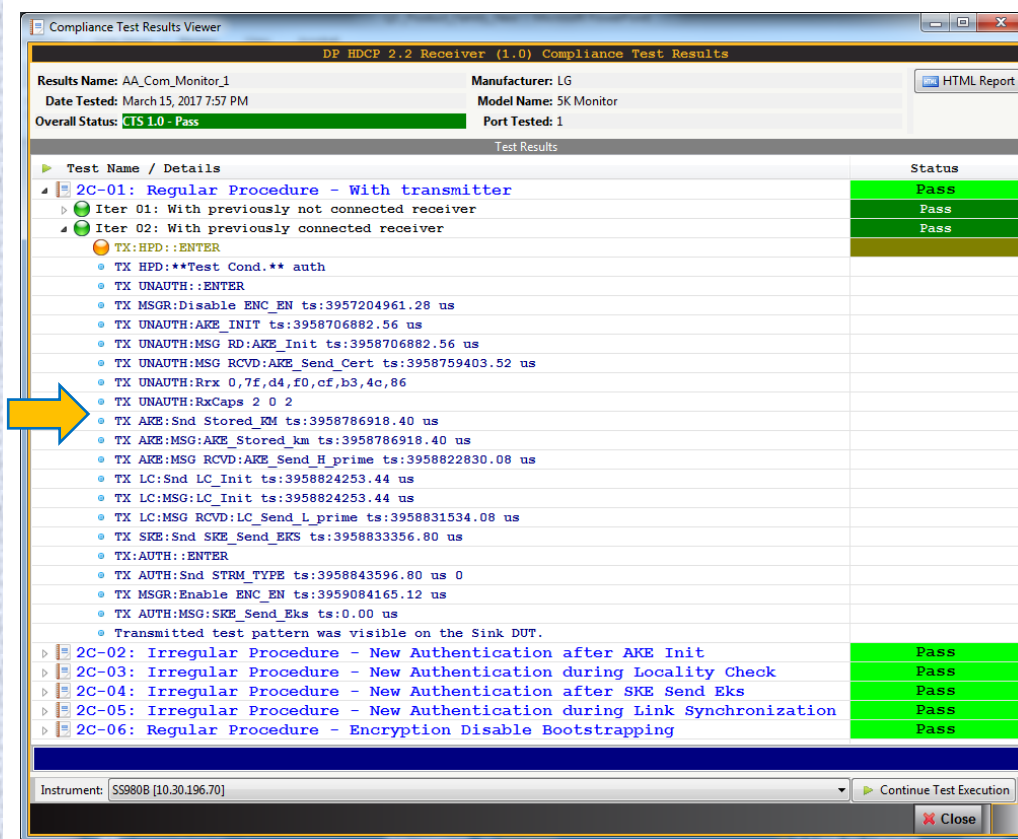
# HDMI 2.1 Sink Testing

## HDCP Compliance Testing



# HDMI HDCP 2.3 Sink Compliance Testing

- ◆ HDMI HDCP 2.3 compliance Testing:
  - ◆ Run HDCP 2.3 sink compliance tests. All tests supported.
  - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
  - ◆ Enables compliance self-testing and/or pre-testing of HDMI devices.
  - ◆ Enables export compliance test results to share with colleagues.



# HDMI HDCP 2.3 Sink Compliance Testing

- ◆ HDMI HDCP 2.3 compliance Testing:
  - ◆ Run HDCP 2.3 sink compliance tests. All tests supported.
  - ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
  - ◆ Enables compliance self-testing and/or pre-testing of HDMI devices.
  - ◆ Enables export compliance test results to share with colleagues.

Compliance Test Results Viewer

HDMI HDCP 2.3 TX (1.0) Compliance Test Results

Results Name: AA\_HDMI\_HDCP\_22\_PC Manufacturer: Nvidia  
Date Tested: May 17, 2016 3:57 PM Model Name: GTX  
Overall Status: **CTS 1.0 - Fail** Port Tested: 1

HTML Report

Test Results

Test Name / Details	Status
1A-01: Regular Procedure: With previously connected Receiver (With stored Km)	Pass
Iter 01:	Pass
1A-02: Regular Procedure: With newly connected Receiver (Without stored Km)	Pass
1A-03: Regular Procedure: Receiver disconnect after AKE Init	Pass
1A-04: Regular Procedure: Receiver disconnect after Km	Pass
1A-05: Regular Procedure: Receiver disconnect after locality check	Pass
1A-06: Regular Procedure: Receiver disconnect after Ks	Fail
Iter 01:	Fail
Clear Ready	
RX HPD Deasserted regular ts:5115282636.80 us	
RX HPD Asserted regular ts:5115432673.28 us	
RX UNAUTH::ENTER	
RX UNAUTH:HDMI/VIDEO Present	
RX UNAUTH:MSG RD:ENC_DIS ts:5115992064.00 us	
RX UNAUTH:RCVD:AKE_Init ts:0.00 us	
RX UNAUTH:**Test Cond.** hpd	
RX AKE:MSG SND:AKE_Send_Cert ts:5117223004.16 us	
RX AKE:MSG RCVD:AKE_No_Stored_km ts:5118022901.76 us	
RX PAIR::ENTER	
RX PAIR:MSG RD:AKE_Send_H_Prime ts:5118037442.56 us	
RX LC:MSG SND:AKE_Send_Pairing_Info ts:5118050856.96 us	
RX LC:MSG RCVD:LC_Init ts:5118052044.80 us	
RX LC:MSG SND:LC_Send_L_prime ts:5118058301.44 us	
RX LC:MSG RCVD:SKE_Send_Eks ts:5118072350.72 us	
RX SKE::ENTER	
RX SKE:MSG RCVD:SKE_Send_Eks ts:5118072350.72 us	
RX HPD Deasserted irregular ts:5118072606.72 us	
RX HPD Asserted irregular ts:5118272634.88 us	
RX UNAUTH:MSG RD:ENC_EN ts:5118292039.68 us	
Encryption Enabled	
1A-07: Regular Procedure: Receiver sends REAUTH REQ after Ks	Pass
1A-08: Irregular Procedure: Rx certificate not received.	Pass

Instrument: SS980B [10.30.196.70] Continue Test Execution

Close



# HDMI HDCP 2.3 Sink Compliance Test - ACA Test Capture Logs

## ◆ HDMI Aux Channel Analyzer Timestamp control:

- ◆ View the ACA transaction files for each HDCP test to confirm failures.
- ◆ View details of any transaction.
- ◆ View time stamps.

The screenshot displays the ACA Data Viewer interface. The main window shows a list of transactions for [HDMI\_HDCP.22] Events: 899 (902). The transactions are listed with their sequence number, type, source/sink, timestamp, and data rate. A yellow arrow points to transaction 827, which is highlighted in blue. Another yellow arrow points from transaction 827 to the detailed view on the right.

**Transaction List (Selected: 827):**

Seq	Type	Source/Sink	Timestamp	Data Rate
813	HDCP	HDMI2-R60	+00:15:44.468466	< 0000 (87.77 kbps)
814	EDID	HDMI2-R60	+00:15:45.899095	R EDID 00 (87.61 kbps)
815	EDID	HDMI2-R60	+00:15:45.899259	< 128 bytes (87.61 kbps)
816	EDID	HDMI2-R60	+00:15:45.912530	R EDID 80 (87.61 kbps)
817	EDID	HDMI2-R60	+00:15:45.912857	< 128 bytes (87.61 kbps)
818	SCDC	HDMI2-R60	+00:15:46.488254	W Config_0 00 (86.54 kbps)
819	SCDC	HDMI2-R60	+00:15:46.492350	W TMD5_Config 00 (86.54 kbps)
820	EDID	HDMI2-R60	+00:15:46.691741	W Segment 00 (87.77 kbps)
821	HDCP	HDMI2-R60	+00:15:46.692068	R HDCP2Version (87.61 kbps)
822	HDCP	HDMI2-R60	+00:15:46.692232	< 04 (87.77 kbps)
823	HDCP	HDMI2-R60	+00:15:46.694571	W AKE_Init (87.77 kbps)
824	HDCP	HDMI2-R60	+00:15:46.697023	R RxStatus (87.77 kbps)
825	HDCP	HDMI2-R60	+00:15:46.907187	< 1602 (87.77 kbps)
826	HDCP	HDMI2-R60	+00:15:46.907187	R Read_Message (87.77 kbps)
827	HDCP	HDMI2-R60	+00:15:46.907187	< AKE_Send_Cert (87.77 kbps)
828	HDCP	HDMI2-R60	+00:15:46.973000	R RxStatus (87.77 kbps)
829	HDCP	HDMI2-R60	+00:15:46.973213	< 0000 (87.77 kbps)
830	HDCP	HDMI2-R60	+00:15:46.984682	R RxStatus (87.77 kbps)
831	HDCP	HDMI2-R60	+00:15:46.984846	< 0000 (87.77 kbps)
832	HDCP	HDMI2-R60	+00:15:46.996151	R RxStatus (87.77 kbps)
833	HDCP	HDMI2-R60	+00:15:46.996478	< 0000 (87.77 kbps)
834	HDCP	HDMI2-R60	+00:15:47.007783	R RxStatus (87.77 kbps)
835	HDCP	HDMI2-R60	+00:15:47.007947	< 0000 (87.77 kbps)
836	HDCP	HDMI2-R60	+00:15:47.009094	W AKE_Stored_km (87.77 kbps)
837	HDCP	HDMI2-R60	+00:15:47.023839	R RxStatus (87.77 kbps)
838	HDCP	HDMI2-R60	+00:15:47.024003	< 2100 (87.77 kbps)
839	HDCP	HDMI2-R60	+00:15:47.024331	R Read_Message (87.77 kbps)
840	HDCP	HDMI2-R60	+00:15:47.024495	< AKE_Send_R_prime (87.77 kbps)
841	HDCP	HDMI2-R60	+00:15:47.030884	W LC_Init (87.77 kbps)
842	HDCP	HDMI2-R60	+00:15:47.043008	R RxStatus (87.77 kbps)
843	HDCP	HDMI2-R60	+00:15:47.043336	< 2100 (87.77 kbps)
844	HDCP	HDMI2-R60	+00:15:47.043664	R Read_Message (87.77 kbps)
845	HDCP	HDMI2-R60	+00:15:47.043827	< LC_Send_L_prime (87.77 kbps)
846	HDCP	HDMI2-R60	+00:15:47.048251	W SKC_Send_Eks (87.77 kbps)
847	HDCP	HDMI2-R60	+00:15:47.062177	R RxStatus (87.77 kbps)

**Transaction Details (827):**

Type: HDCP  
Start Time: +00:15:46.907842  
Duration: 54.067 msec  
Maximum I2C Rate: 87.77 kbps  
Read, 534 bytes  
Register: 80h  
Name: Read\_Message  
Message: AKE\_Send\_Cert (534 bytes)  
msg\_id: 3  
cert\_rx: [4175..0]  
Receiver ID: 8C 23 BA D5 A6  
Receiver Public Key:  
C5 3B FC EC 4E 2A 42 EA 71 76 F4 B8 90 7A EC 7B  
F5 78 07 11 97 35 5C D6 F8 09 30 D3 DB 4C 91 C4  
7D 82 CE F6 7D 7F 22 A1 1D A7 9F 6F C1 4A 52 16  
AE 09 5A CC 59 DF 5F C2 07 19 D8 A7 02 D0 4C 85  
B8 16 F4 DA 3A 12 8B 00 84 E1 D3 2E 2C EA 76 05  
83 F8 12 B0 74 E6 B9 CB 5B DB BB FB 39 A3 26 4A  
DF B9 E9 5A BD DF 97 89 73 63 38 2B 95 1D 52 84  
CA 1F 07 46 F1 14 36 1A 3F 61 BE 2E C2 E2 75 B3  
01 00 01  
RESERVED: 00 00  
DCC LLC Signature:  
28 A8 50 53 80 72 16 76 A3 EB 07 D7 FC F7 A7 DB  
38 72 33 D5 26 76 87 64 3A D1 A4 45 86 6D 86  
9D 58 B4 3E 16 CD F8 B7 24 D7 74 F9 4E 76 C5 10  
1B D0 E8 4B 53 33 1A 6D 72 E2 3A 8A 79 FE BC FC  
52 9C 21 8E 4D 9F 8A 33 2E BA 8F B4 69 36 C4 F0  
DF BC 47 6B 5D 3B 4D 72 62 F3 19 B2 24 E5 EE 61  
4A DF 57 82 1F 03 23 DB DB 41 0B 25 79 28 FE A6  
72 ED 4D 42 1F D8 7F 31 A4 9A 97 97 8E 13 10 A5  
0D 00 EB 48 97 71 5E 5C B5 1A 81 86 6D DB A9 97  
CC 9A 2C 40 B8 1B 59 50 7B 2A 0B 46 EF DE C3 E2  
FF 8E AD E7 9A 0E FC D2 D2 1C 9E 35 25 E2 C2 22  
F7 CC 4C FE B2 0E C2 56 46 57 9F F5 1A 1A 32 FC  
5E E1 58 12 57 48 47 33 96 4C 0B 99 E7 C3 5E 6C  
61 E0 DD B6 23 BE 3E 97 82 4F 11 B4 70 86 27 B6  
A8 C2 95 C1 F5 EC 39 8F EC E3 7E FD 01 36 EE 0A  
B2 F0 95 01 A4 74 92 F5 3C 10 9B 5B B9 60 61 FC  
BC 68 0C 07 DA 72 C7 74 B6 15 75 B1 65 A7 BF F3

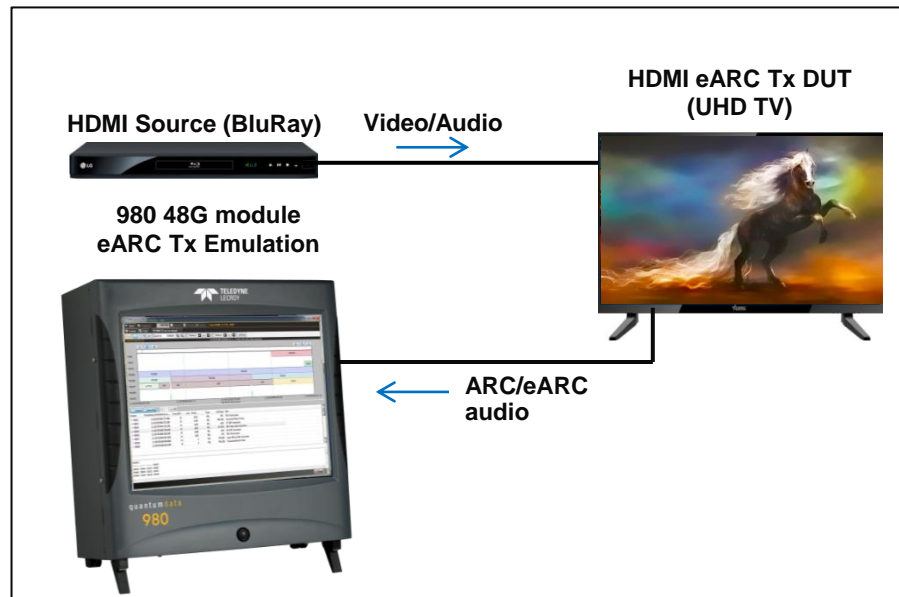
# HDMI 2.1 eARC Testing

## Enhanced Audio Return Channel



# HDMI eARC Tx Testing

- ◆ HDMI 2.1 eARC Testing:
  - ◆ Verify eARC Tx (TV) for common mode and differential mode operation.
  - ◆ Run eARC common and differential mode compliance tests for Tx devices. Full list of tests supported.



# HDMI eARC Tx Testing

## ◆ HDMI 2.1 eARC Testing:

- ◆ Verify eARC Tx (TV) for common mode and differential mode operation.
- ◆ Run eARC common and differential mode compliance tests for Tx devices. Full list of tests supported (only partial list shown right).



# HDMI eARC Tx Testing

## ◆ HDMI 2.1 eARC Testing:

- ◆ Verify eARC Tx (TV) for common mode and differential mode operation.
- ◆ Run eARC common and differential mode compliance tests for Tx devices. Full list of tests supported.
- ◆ Provides detailed Test Results with Pass/Fail and details for each subtest.
- ◆ Enables compliance self-testing and/or pre-testing of eARC devices.
- ◆ Enables export of compliance test results to share w/ colleagues.

Compliance Test Results Viewer

eARC Source (1.0) Compliance Test Results

Results Name: AA\_eARC\_Tx\_Complete\_MB      Manufacturer: qd  
Date Tested: August 13, 2018 9:02 AM      Model Name: 980  
Overall Status: **CTS 1.0 - Fail**      Port Tested: 1

HTML Report

Test Results

Test Name / Details	Status
▶ HFR5-1-20: eARC Discovery With COMMA Width Margining	Pass
▶ HFR5-1-21: Command Behavior With Bit Time Margining	Pass
▶ HFR5-1-22: TX gets <NACK> indicating eARC RX Busy	Pass
▶ HFR5-1-23: TX gets Common Mode Slow Response	Pass
▶ HFR5-1-24: eARC TX gets Timeout during Heartbeat	Pass
▶ HFR5-1-25: eARC TX gets Heartbeat Disconnect	Pass
▶ HFR5-1-26: eARC TX gets HPD LOW Disconnect	Pass
▶ HFR5-1-50: eARC TX Responds <RETRY> to Read Data Packet With Uncorrectable ECC Error	Pass
▶ HFR5-1-55: eARC TX gets Heartbeat Failure during Discovery	Pass
▶ Iter 01:	Pass
▶ 01: HFR5 1 55 1: No response to <eARC Write>	Pass
▶ HFR5-1-35: eARC TX Reads Capabilities Data Structure at startup	Fail
▶ Iter 01:	Fail
▶ 01: HFR5 1 35 1: Verify CAP_CHNG_CONF behavior	Fail
• Iteration 1, verify CAP_CHNG_CONF	
• Collected 3523 events	
• Analyzed 3523 events	
• DUT took 72.013875ms from HPD=1 to issue heartbeat (maximum: 500ms)	
• DUT sent HB after 4 COMMA ONs	
• DUT set CAP_CHNG_CONF=1 in 353.7651ms (200ms max)	
• DUT set CAP_CHNG_CONF=0 in 202.371275ms (200ms max)	
• DUT started reading Capabilities Data Structure in 424.05195ms (2s max)	
▶ HFR5-1-36: eARC TX Re-reads Capabilities Data Structure when CAP_CHNG->1	Fail
▶ HFR5-1-28: eARC TX 2-channel LPCM Audio Packet Structure	Pass
▶ HFR5-1-29: eARC TX Multi-Channel 2-channel layout LPCM Audio Packet Structure	Pass
▶ HFR5-1-56: eARC TX Multi-Channel 8-channel layout LPCM Audio Packet Structure	Pass

Open ACA Data

Instrument: S59808 [10.30.196.240]      Continue Test Execution      Close



# HDMI eARC Common Mode Configuration Sequence

- ◆ HDMI 2.1 eARC Testing:
  - ◆ Verify eARC common mode connection sequence using Aux Channel Analyzer (ACA) utility.
  - ◆ Enables export of ACA eARC Common Mode transactions to share w/ colleagues.



ACA Data Viewer

Open Close Export Options Filter Find

[My\_eARC\_Log\_1] Events: 28 (54)

Index	Type	Channel	Time	Description
0	EARC	HDMI-R10	+06:37:28.021241	Invalid Sequence
1	EARC	HDMI-R10	+06:37:28.069262	Read EARC_RX_STAT 00
2	EARC	HDMI-R10	+06:37:28.069813	Write EARC_TX_STAT 81
3	EARHB	HDMI-R10	+06:37:28.116296	Heartbeats 166
4	SV	HDMI-R10	+06:37:36.078772	SV Falling Edge
5	SV	HDMI-R10	+06:37:37.884404	SV Rising Edge
6	EARCM	HDMI-R10	+06:37:37.885490	Comma ON: 9.999 ms
7	EARCM	HDMI-R10	+06:37:37.905489	Comma ON: 10.000 ms
8	EARCM	HDMI-R10	+06:37:37.925489	Comma ON: 10.000 ms
9	EARC	HDMI-R10	+06:37:37.939303	Read EARC_RX_STAT 18
10	EARC	HDMI-R10	+06:37:37.939853	Write EARC_TX_STAT 99
11	EARHB	HDMI-R10	+06:37:37.985256	Heartbeats 1
12	EARC	HDMI-R10	+06:37:38.033313	Read EARC_RX_STAT 00
13	EARC	HDMI-R10	+06:37:38.033860	Write EARC_TX_STAT 81
14	EARC	HDMI-R10	+06:37:38.081215	Read CAPS 00h L=8
15	EARCD	HDMI-R10	+06:37:38.082492	Cap Data: L=8
16	EARC	HDMI-R10	+06:37:38.082526	Read ERX_LATENCY 00
17	EARHB	HDMI-R10	+06:37:38.083075	Heartbeats 27
18	EARC	HDMI-R10	+06:37:39.392340	Read EARC_RX_STAT 00
19	EARC	HDMI-R10	+06:37:39.392909	*Write EARC_TX_STAT 81
20	EARHB	HDMI-R10	+06:37:39.440367	Heartbeats 37
21	EARC	HDMI-R10	+06:37:41.228225	Read EARC_RX_STAT 00
22	EARC	HDMI-R10	+06:37:41.228761	Write EARC_TX_STAT 00
23	EARHB	HDMI-R10	+06:37:41.277215	Heartbeats 43
24	EARC	HDMI-R10	+06:37:43.341254	Read EARC_RX_STAT 00
25	EARC	HDMI-R10	+06:37:43.341835	Write EARC_TX_STAT 83
26	EARHB	HDMI-R10	+06:37:43.389271	Heartbeats 83
27	EARC	HDMI-R10	+06:37:47.396808	Write

Type: eArc  
Start Time: +06:37:37.939303  
Duration: 516 us

Read EARC\_RX\_STAT 18

0x00: EARC\_RX\_STAT

Bit	Name	Value	Description
0	EARC_HPD	N(0)	
1		0	Reserved
2		0	Reserved
3	CAP_CHNG	Y(1)	
4	STAT_CHNG	Y(1)	
5		0	Reserved
6		0	Reserved
7		0	Reserved

Packet Sequence:

Index	Type	Channel	Time	Description
001:	M C	01h Read	+0 us	
002:	S C	04h Ack	+24 us	
003:	M D	74h	+34 us	
004:	S C	04h Ack	+24 us	
005:	M D	D0h	+34 us	
006:	S C	04h Ack	+24 us	
007:	M C	10h Cont	+34 us	
008:	S D	18h	+24 us	
009:	M C	20h Stop	+33 us	
010:	S C	04h Ack	+24 us	

(M/S = Master/Slave, C/D = Command/Data)

9: Read EARC\_RX\_STAT 18

