

VIDEO TEST INSTRUMENTS

LINK LAYER COMPLIANCE TEST APPROVED BY VESA

Introducing the latest video test instrument from Quantum Data, the 882E, which now offers a DisplayPort interface. The DisplayPort transmitter (source) interface is an optional feature of the model 882E test instrument that can deliver blazing fast video at pixel rates up to 268MHz. One (1), 2, and 4-lane configurations are supported at per-lane rates of 1.62Gb/s and 2.7Gb/s. The DisplayPort transmitter supports HDCP and link layer compliance testing of sink devices (displays). The DisplayPort receiver option emulates a DisplayPort sink device and supports link layer compliance testing of DisplayPort source devices. Auxiliary channel transactions can be monitored with the Auxiliary Channel Analyzer (ACA).





DisplayPort analyzer depicted in illustration above

KEY FEATURES + BENEFITS

DisplayPort Tx Interface

Supports 1, 2 and 4 lanes @ 1.62 GB/s and 2.7 Gb/s per lane provides 10 bits/component up to 268MHz pixel rate.

DisplayPort Rx Interface

Supports 1, 2 and 4 lanes @ 1.62 GB/s and 2.7 Gb/s per lane provides 10 bits/component up to 268MHz pixel rate.

HDCP Test

Supports HDCP production and compliance tests for displays.

Link Layer Compliance Test

Approved by VESA

Supports link layer compliance testing for source and sink devices.

Auxiliary Channel Analyzer (optional)

Real time logging of Auxiliary Channel (link layer transactions, DPCD, HDCP and EDID).

central administration/network control

Update and configure all networked instruments from a single computer. Fully control instrument from any network location with web browser or Telnet client.

graphics SDK

Create complex patterns based on your specifications using C++ software development kit.

comprehensive timing + patterns

Include extensive library of standard timings and patterns. Add your own custom timings and patterns.

local pattern storage

Store multiple custom images (.bmp, .jpg and .png) images in instrument.

easy to use

Access powerful features easily using intuitive user interface.

multiple configurations

Save and restore different instrument configurations for different users or applications.

HDCP Testing	
·	Authentication and encryption of
	uncompressed DisplayPort video sinks
HDCP Compliance Testing	
(optional)	For testing sink devices
Link Layer Compliance Test	For testing source devices
(optional)	For testing sink devices
Auxiliary Channel Analyzer	Real time logging of Auxiliary Channel (link layer
(optional)	transactions, DPCD, HDCP and EDID)
EDID Read	Auto-configuration of generator format list
Data channels	I2C per VESA E-DDC
Physical	DDC2B, E-DDC & DDC/CI
Protocols	(reads E-EDID Ver 1.4)
EDID Testing	Reads EDID from display and
Ÿ	presents as displayed image
Scrolling Image Test (ImageShift) All interfaces	Scroll any static image
Special Sync Tool	Trigger scope or inspection camera
	anywhere in video
Formats	Over 580 formats for testing IT, CE, military
Standard formats	and other display test applications
	Graphical format editor for creating custome formats
Custom formats	
Patterns	Custom object (.o) files, BMP, JPEG, PNG
Pattern file types	Over 320 standard static and dynamic
Standard patterns	images included for testing CRTs and FPDs
	Graphics SDK to create complex patterns
Custom patterns	15 MB
Internal data storage	
Test Sequences	Create test sequences with unlimited
	number of steps; each step defines a
	video format, image, sync, gating and
	duration (0.1 sec to 24 hours, or frames)
	Create custom images applications using Quantum
Software Development Kit	Data SDK (includes API documentation, sample
(SDK)	application & source)

DisplayPort TX Interface	
Connectors	Box to box external per spec
Video	
Lanes	1, 2, 4 (user specified)
Lane data rate	1.62 Gb/s, 2.7 Gb/s (user specified)
Bit depths	6, 8, 10
Colorimetry	RGB, YCbCr
Sampling	4:4:4
Formats	VESA: DMT and CVT
Hot Plug	1) 0.5ms->1.0ms
	2) 2ms
Aux channel Mode	Native for DPCD link configuration
	2) I2C for EDID reads
Pixel Clock	2) 120 101 EDID Teaus
	Maximum: 268MHz
Frequency range	
Step	Less than 0.1 Hz
Accuracy	50 ppm (electronically adjustable to
	<5 ppm with external frequency
	counter)
Horizontal Timing	
Frequency range (kHz)	Maximum: 300 kHz
	Minimum: 1 kHz
Total pixels (max)	65,534
Active pixels (max)	4096
Blank pixels (min)	12 (minimum)
Step pixels	1
Vertical Timing	
Frequency range	Maximum: 250 Hz
rrequerity range	Minimum: 23 Hz
Total lines (max)	2048 progressive, 8,191 interlaced
	and segmented
Active lines (may)	
Active lines (max)	2048
Blank lines (min)	1 to Total-1
Step lines	1
Scan types	Progressive, interfaced, segmented
Video Memory	
Size	16,384,000 pixels at 32-bits/pixel
	32,768,000 pixels at 8-bits/pixel
Maximum width	16,384 pixels at 32 bits/pixel
	16,384 pixels at 8 bits/pixel
Color depth	32 (24-bit TrueColor) up to 268 MHz
	8 bits up to 268 MHz
Administration	
Physical user interface (selec	ction keys and display)
Control interfaces	RS-232 serial AT 10/100 BaseT
	Ethernet (TCP/IP, FTP, Telnet) GPIB
Browser-based virtual contro	
from any network location	. ps. to manage
PCMCIA slot	Compact Flash card to boot generator,
I OIVIOIA SIUL	
	backup generator configuration, copy
	generator configuration to other generator
	and store patterns
General Specifications	
Size (mm)	330 W, 87 H, 284 D
Humidity	30 to 80% RH (non-condensing)
Trainiaity	
	0 to 40° C
Operating temp.	0 to 40° C
Operating temp. AC Mains Frequency	0 to 40° C 47 to 63 Hz

882E DisplayPort Compliance Test Solutions

The 882E Display Port test instrument provides powerful aux channel related test features including link layer compliance testing and HDCP compliance testing as well as an aux channel nel protocol analyzer for capturing link training, HDCP and EDID transactions.

Link Layer Compliance Testing

The 882E offers a VESA approved link layer compliance test. The compliance tests can be configured and run through a graphical user interface. Tests can be run individually or as a complete test suite. You can pick and choose which tests run and how often they are repeated in any one run of the test suite. Once the test is complete, a comprehensive report is provided which shows both a summary section and a detailed section as shown below.

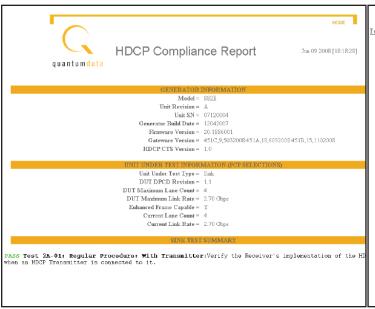


Link Layer Compliance Test Interface

Link Layer Compliance Report

HDCP Compliance Testing

The 882E provides an approved HDCP compliance test application for DisplayPort. Tests can be run individually through the command line or as a complete test suite through the front panel. Once the test is complete, a comprehensive report is provided which shows both a summary section and a detailed section as shown below.



Test Results [0] DUT has asserted HPD. 0.4096 sec [1] DUT is HDCP Capable (Bcaps - 0x01). 0.4096 sec All bytes (133) at the HDCP Reserved DPCD Address (0z6803B) are zero All bytes (133) at the HILLY Reserved DPU Address (USb013) at 00068038: 0x00, 0.4096 sec All bytes (15) at the HDCP KSV Fifo DPCD Address (0x6802C) are zero. 0006802C: 0x00, 0x 0.4096 sec Bksv (MSB->LSB) = 0xC77F40C668 Bcaps = 0x01 An (MSB->LSB) = 0x853FF01CE45EE7EB Aksv (MSB->LSB) = 0x866FDD320A 0.4096 sec

HDCP Compliance Test Report - Summary

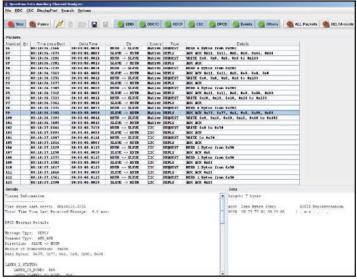
HDCP Compliance Test Report - Detail

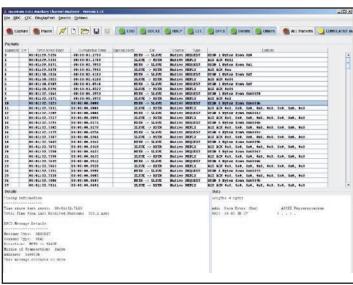
882E DisplayPort Auxiliary Channel Test Solutions

Auxiliary Channel Analyzer

The 882E provides an optional auxiliary channel analyzer for monitoring protocol transactions occurring over the auxiliary channel.

You can monitor the aux channel during link training in normal operation, or during link layer compliance testing or HDCP compliance testing. Transactions are parsed out in the "Details" section. This enables you to view the register values in human readable text as shown below.

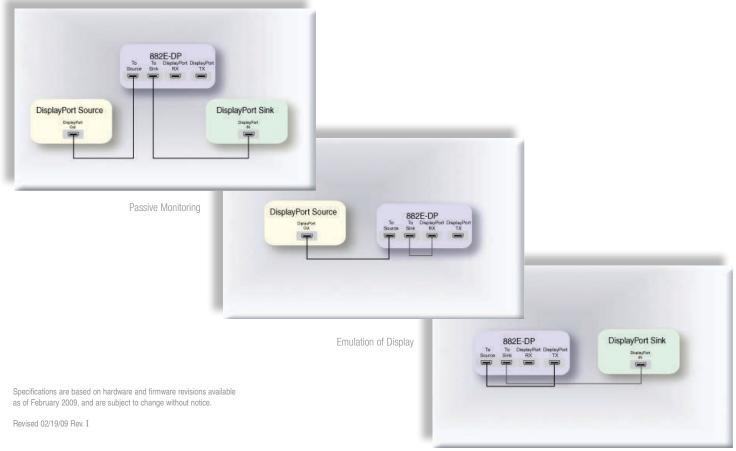




Link Layer Transactions

HDCP Transactions

There are three configurations for monitoring the DisplayPort transactions. You can monitor the aux channel transactions either while the 882E is emulating a DisplayPort sink for testing a source device, or while emulating a DisplayPort source device for testing a sink device. You can also monitor passively between a DisplayPort source and sink device. These configurations are depicted below.



Emulation of Source