

1. Noise Sequence

The pseudo random pixel generation is the same as described in the file DVI_Test_Pn.pdf.

2. Synchronization Sequence & Error Definition

The proposed synchronizing sequence is as follows:

```

Channel #           ----- 2 ----- ----- 1 ----- ----- 0 -----
Component           ----- R ----- ----- G ----- ----- B -----
Component Bit #     7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0 7 6 5 4 3 2 1 0
                    MSB                                     LSB
                    |                                       |
Rx_Clock(0)         s s s s s s s s s s s s s s s s s s s s s s s s s s
Rx_Clock(1) "MagicA" 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
Rx_Clock(2) "MagicB/Op/SeedH" 0 0 0 0 0 0 0 a b c d e f g h i j k l m n p q r
Rx_Clock(3) "SeedL"  A B C D E F G H I J K L M N P Q R S T U V W Y Z

```

```

Lx_SR_Bit #        3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0 0
                   0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0
                   |               <-- shift effectively 24 at a time               |
Lx_SR_Clock(0)    x x x x x x x s s s s s s s s s s s s s s s s s s s s s s s
Lx_SR_Clock(1)    x x x x x x x x x x x x x x x x x x x x x x x x x x x x x
Lx_SR_Clock(2)    x x x x x x x x x x x x x x x x x x x x x x x x x x x x x
Lx_SR_Clock(3)    k l m n p q r A B C D E F G H I J K L M N P Q R S T U V W Y Z

```

s = a bit of some value that IS checked

x = a bit that doesn't matter

MagicA = 0

MagicB = 0 0 0 0 0 0 0

Op = a b c d e f g h i j

SeedH = k l m n p q r

SeedL = A B C D E F G H I J K L M N P Q R S T U V W Y Z

An error is defined as:

$Rx_Clock(z) \neq Lx_SR_Clock(z)$

where $Rx_Clock(z)$ and $Rx_Clock(z+1)$ are not "MagicA" and "MagicB/Op/SeedH", respectively.

3. DE Sensitivity Option

Normally, the pipeline should be advanced by one position for each pixel clock. Optionally, the shift register can be setup to shift only while DE is true. An Op code of a=0, b=0, c=0, d=0, e=0, f=0, g=0, h=1, i=1, and j=1 is received, then the shift register must not shift while DE is false.

4. VS-DE Reset Option

In cases where a synchronizing re-seed event is never sent by the source, an alternative reset method is available to reset the noise at the beginning of each field. This is the same as the method outlined in the DDWG Electrical Test Working Group's DVI Test & Measurement Guide (Revision 1.0). The first DE rising edge after VSYNC is used as a re-seed load signal.

5. Interlace

Noise values always proceed in time order – not necessarily screen order. Therefore, it may be necessary to skip lines, when rendering noise into a frame buffer that is sourcing interlaced video.