DVI PSUEDO-NOISE PIXEL SEQUENCE PROPOSAL

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1 PSUEDO-NOISE PIXEL SEQUENCE GENERATOR

1.1 Background

The DVI 1.0 specification describes testing the channel with a pseudo random data pattern with a repeat cycle of at least 2^{23} - 1. The specification is not specific about how this is to be achieved or exactly what should not repeat for 2^{23} - 1 cycles. In order to facilitate interoperability testing, it is desirable to specify the specific pattern to be used. Standardization on the sequence to use will enable any vendor to provide a method for testing link quality without additional expensive test equipment.

The most desired pseudo random pattern is one that randomizes both the pixels to be transmitted and the bits to be transmitted. Alternatives such as providing a random bit pattern that is phase shifted to each of the bits within a pixel have an inherent high degree of correlation. Since minimizing correlation is the purpose of a pseudo random pattern, it is a simple conclusion that the phase shifted solution has not achieved minimal correlation.

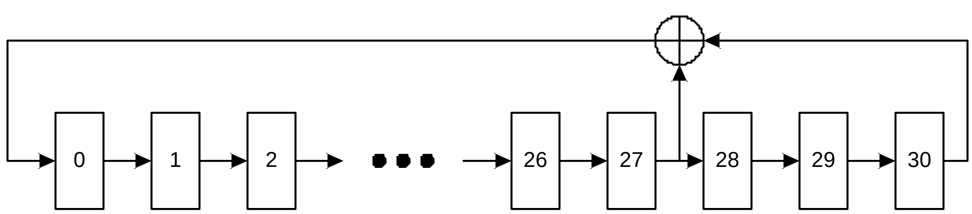
This pseudo random set of pixels will be referred to as a Pseudo-Noise Pixel Sequence (PNPS). An additional requirement for the PNPS is a simple implementation that can be realized with no more than one Exclusive-OR or Exclusive-NOR gate between flip-flops running at the pixel clock frequency. This minimizes the speed demands for implementations allowing the PNPS generator run at speeds well in excess of 165 MHz.

1.2 Building Block: Single Shift Linear Feedback Shift Register

It is desirable to allow for sequences that provide a non-repeating sequence for several seconds. The metric used in developing this test was 10 seconds at 165MHz. Looking at standard sequences, the simplest generator polynomial (i.e. least terms) that can generate a sequence of at least this length is:

$$f(x) = 1 + X^{28} + X^{31}$$

This sequence can be represented as a 31 bit, single shift, Linear Feedback Shift Register (LFSR). The LFSR looks like:



This sequence can be represented with the following equations:

```
r0  = r27 ⊕ r30
r1  = r0
r2  = r1
•
•
•
r29 = r28
r30 = r29
```

The length of this sequence is $2^{31} – 1$ and repeats every 13 seconds at a 165MHz pixel rate.

1.3 Pixel Shift Linear Feedback Shift Register

Taking the low order 24 bits of the single shift LFSR as pixel data, it is necessary to shift the generator 24 times in each pixel clock cycle. The 24-shift sequence can be represented by the following equations:

```
r0  = r4  ⊕ r7
r1  = r5  ⊕ r8
r2  = r6  ⊕ r9
r3  = r7  ⊕ r10
r4  = r8  ⊕ r11
r5  = r9  ⊕ r12
r6  = r10 ⊕ r13
r7  = r11 ⊕ r14
r8  = r12 ⊕ r15
r9  = r13 ⊕ r16
r10 = r14 ⊕ r17
r11 = r15 ⊕ r18
r12 = r16 ⊕ r19
r13 = r17 ⊕ r20
r14 = r18 ⊕ r21
r15 = r19 ⊕ r22
r16 = r20 ⊕ r23
r17 = r21 ⊕ r24
r18 = r22 ⊕ r25
r19 = r23 ⊕ r26
r20 = r24 ⊕ r27
r21 = r25 ⊕ r28
r22 = r26 ⊕ r29
r23 = r27 ⊕ r30
r24 = r0
r25 = r1
r26 = r2
r27 = r3
r28 = r4
r29 = r5
r30 = r6
```

The final definition needed is the exact mapping of the shift register bits to the pixel data.

```
RED[7:0] = r[23:16]
GRN[7:0] = r[15:8]
BLU[7:0] = r[7:0]
```

```
PIXEL[23:0] = { RED[7:0], GRN[7:0] BLU[7:0] } = r[23:0]
```

The accompanying file, “PN_31_24.txt” lists the first 10000 states of the generator sequence for development purposes.